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MULTIPORT MULTIPLEX PROGRAM

AIRESEARCH MANUFACTURING COMPANY OF CALIFORNIA
2525 WEST 190TH STREET
TORRANCE, CALIFORNIA 90509

FEBRUARY 1975

FINAL REPORT: APRIL 1974 - FEBRUARY 1975

AIR FORCE ARMAMENT LABORATORY
AIR FORCE SYSTEMS COMMAND • UNITED STATES AIR FORCE
EGLIN AIR FORCE BASE, FLORIDA

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Image Coding Differential PCM Coding

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A video digital encoder/decoder has been developed and constructed that will encode, transmit, and reconstruct high-quality, real-time television pictures.

The analog television signals are encoded into digital format using a differential pulse code modulation (DPCM) technique resulting in a transmitted data rate of 3 bits per picture element. This type of coder has potential application in areas where the signal-to-noise advantages of digital data transmission

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20. ABSTRACT (Continued)

bandwidth of conventional pulse code modulation (PCM) coders that require between 6 and 8 bits of data per television picture element.

DPCM coders compare the present sample picture element with the preceding sample picture element, and only the difference is digitally encoded and transmitted. Digital accumulators are utilized to hold the previous picture element instead of analog integrators. This ensures perfect tracking between the encoder and decoder and eliminates the need for precision components and lengthy calibration procedures.

The television signal is sampled at a rate of 10 MHz and digital data is transmitted at a rate of 30 Mbits per second. Error propagation is controlled. Data transmission errors are corrected and dc operating levels are restored at the beginning of every horizontal television line. Fabrication of the encoder and decoder utilized high-speed, commercially available, emitter-coupled-logic (ECL) integrated circuits installed on low-impedance, wire-wrap logic cards.

PREFACE

This report documents work performed during the period from April 1974 to February 1975 by AiResearch Manufacturing Company, 2525 West 190th Street, Torrance, California 90509, under Contract F08635-74-C-0097 with the Air Force Armament Laboratory, Armament Development and Test Center, Eglin Air Force Base, Florida 32542. Mr. Claude M. Connell (DLJA) managed the program for the Armament Laboratory.

This report has been reviewed and is approved for publication.

FOR THE COMMANDER:

William F. Brockman

WILLIAM F. BROCKMAN, Colonel, USAF
Chief, Munitions Division

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SECTION I

INTRODUCTION

This final report summarizes the work performed under Contract F08635-74-C-0097, multiport multiplex group program. The work statement for the multiport multiplex group specified design, development, and fabrication of a breadboard multiplexer, transmission medium, and demultiplexer for a high-frequency multiplex system (see Figure 1). Design specifications for the multiplex channels were:

(a) 7.5-MHz bandwidth, Composite Electronics Industries Association (EIA) video

(b) 12-channel analog input conditioning for 1-MHz bandwidth signal

(c) 32 input channels for discrete or digital signals

(d) Design and development of a full duplex video transmission link.

As a result of standardization by the Air Force on the MIL-M-1553 multiplex requirements and concentration on video data transmission and recovery, the program was rescoped to design, develop, and fabricate the video encoder/decoder (3-bit DPCM) and a bidirectional data transmission link.

Section 1 is a summary of results and includes fabrication, testing, encoder/decoder performance, conclusions, and recommendations. The design approach is discussed in Section II; Section III presents theory and operation. Breadboard system fabrication is discussed in Section IV. Image coding and digital data link development information is presented in the appendixes.

1.1 FABRICATION

The bidirectional transmission link operating at 100 MHz and the video encoder/decoder were fabricated and tested. Off-the-shelf components were employed in the fabrication of the encoder/decoder, and standard laboratory packaging was used.

1.2 TESTING AND TEST RESULTS

1.2.1 Video Transmission Digital Data Link

A full duplex digital data transmission link was fabricated and tested using coaxial cable with simultaneous bidirectional input of 100 Mbits/sec. Data were transmitted and recovered. The prototype video digital data link is shown in Figure 2. The transmission system comprises two receivers, two transmitters, two bidirectional couplers, and the RG-14A/U coaxial cable transmission link.

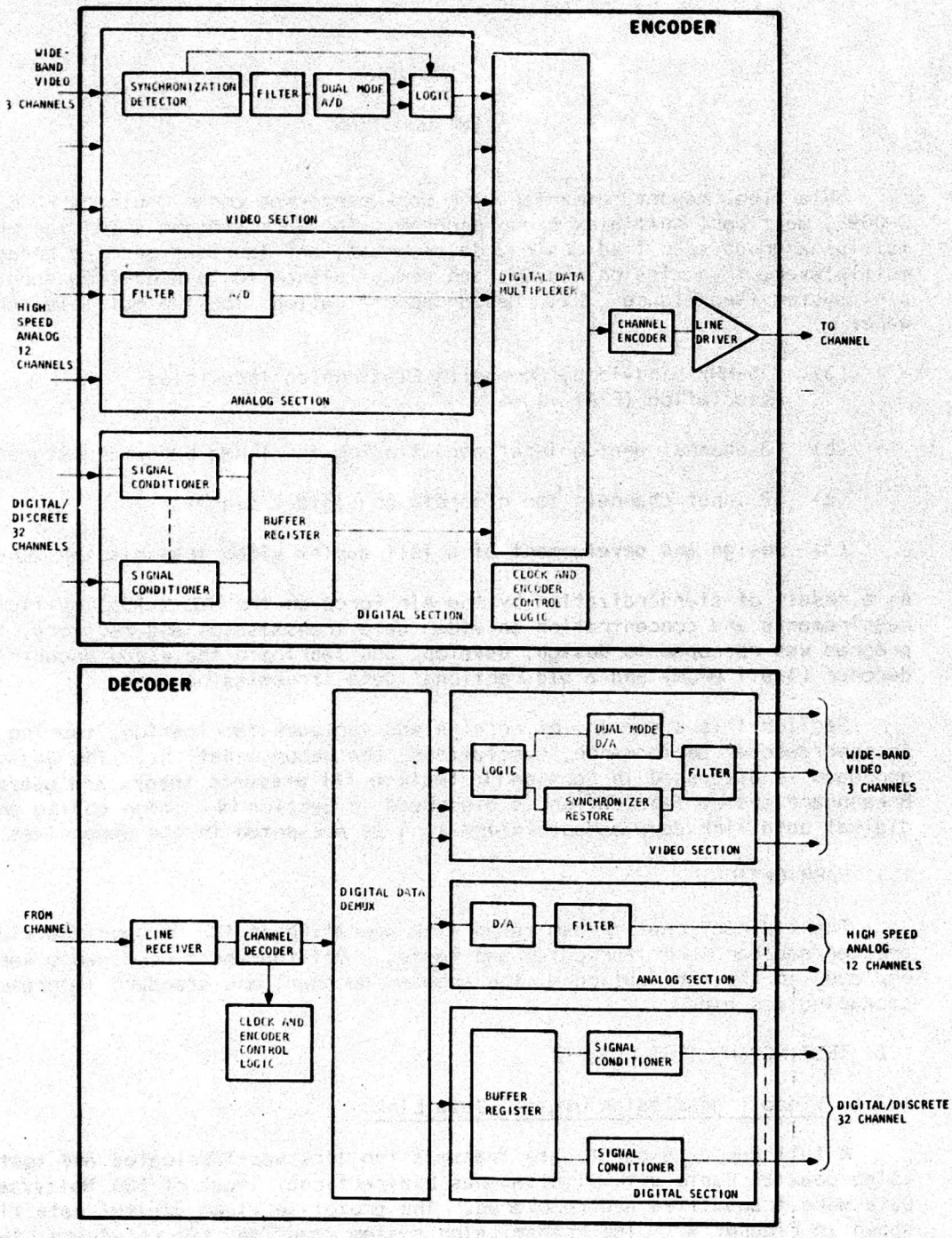

Figure 1. Signal Flow Multiplexer Encoder Inputs to Decoder Outputs

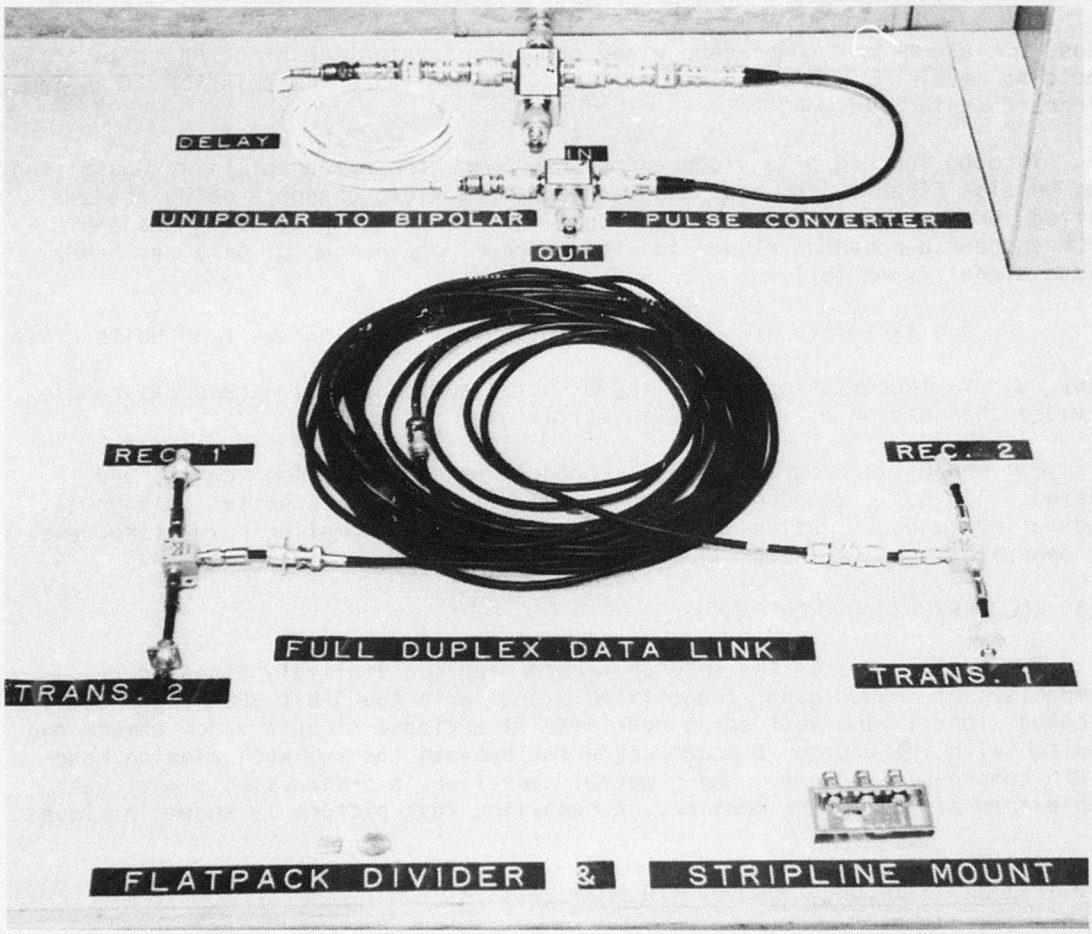

Figure 2. Prototype Video Digital Data Link

1.2.2 High-Frequency Analog/Digital (A/D) Converter

A high-frequency analog/digital converter was tested at a frequency of conversion of 1 μsec/6 bits. The A/D converter provided complete accuracy and settling time performance required by the work statement.

1.2.3 Video Encoder/Decoder

The purpose of the video encoder/decoder was to demonstrate that high-frequency, digital, bidirectional video data transmission employing bandwidth-compressed techniques can result in quality video pictures being recovered and displayed. Considering a normal digitizer that has an 8-bit conversion and is sampled at a rate of 2 samples/cycle, the number of data bits transmitted for a 5-MHz video signal would be as follows:

$$8 \text{ bits/sample} \times 2 \text{ samples/cycle} \times 5 \times 10^6 \text{ cycles/sec} = 80 \text{ Mbits/sec}$$

Thus, for a non-data-compressed video channel, a data link of 80 Mbits/sec would be required. This would normally fill available transmission links for aircraft application.

Through the use of a video encoder/decoder, the number of bits transmitted can be significantly reduced, resulting in more video channels being transmitted for the same grade transmission link. As an example, using the 3-bit DPCM encoder/decoder developed for the program, the number of bits per 5-MHz video signal is as follows:

$$3 \text{ bits/sample} \times 2 \text{ samples/cycle} \times 5 \times 10^6 \text{ cycles/sec} = 30 \text{ Mbits/cycle}$$

Thus, a data transmission link with 90-Mbits/sec transmission rate can handle 3 video channels on a time division multiplexed basis.

For the Eglin program, a video encoder was designed, fabricated, and tested. The basic encoder operates in a 3-bit DPCM (differential pulse code modulation) mode. Testing was conducted at variable sampling rates (frequency of operation) and variable bit encoding levels.

1.3 ENCODER/DECODER PERFORMANCE

The performance of the encoder/decoder was qualitatively assessed by comparison of the original transmitted signal with the 3-bit DPCM video compressed signal. The test setup consisted of a closed circuit video camera and monitor with the encoder/decoder connected between the two when viewing bandwidth compressed signals. Under normal operation, a 5-MHz video signal was cable-transmitted to the monitor. A resulting test picture is shown in Figure 3.

1.3.1 1 Bit - Encoded/Decoded (10 MHz)

The encoder/decoder was modified to operate as a 1-bit encoder/decoder. A photograph from a bandwidth-compressed signal using the 1 bit/sample DPCM (commonly referred to as delta modulation) is shown in Figure 4. The picture

Figure 3. Normal Operation, 5-MHz Video Signal Transmission

Figure 4. 1-Bit Encoded/Decoded DPCM at 10-MHz Sample Rate

indicates both granularity and inability to track the sharp edges of a highly contrasted area. When using the DPCM mode, these two phenomena occur and are referred to as:

(a) Granularity

(b) Slope overload

Granularity results from the threshold at which a 1 bit will be transmitted. The threshold corresponds to a finite change on the gray scale or resolution of the adjacent picture elements. By increasing the resolution (decreasing the voltage threshold), the granularity will be reduced. This reduction, however, results in inability to track a highly changing contrast area (see Figure A-4 of Appendix A). The tradeoff is to minimize both of these effects by optimizing the voltage threshold level. A typical aircraft system video picture (Figure 5) supplied by Eglin Air Force Base provides a comparison to the 1-bit DPCM. This comparison shows that 1 bit DPCM operating at 10 MHz is probably sufficient for the stores management application.

1.3.2 2-Bit Encoded/Decoded DPCM (10 MHz)

The encoder/decoder was modified to perform in a 2-bit DPCM mode. The results of this modification are shown in Figure 6. A comparison of the original (Figure 3) and the bandwidth-encoded picture shows negligible degradation.

1.3.3 3-Bit Encoded/Decoded DPCM (10 MHz)

Results of the Eglin encoder/decoder acting as a 3-bit DPCM system are shown in Figure 7. The quality of the picture is actually enhanced by the 5-MHz bandwidth limit, which eliminates spurious high-frequency signals.

1.3.4 3-Bit Encoded/Decoded DPCM (2 MHz)

The encoder/decoder was modified to operate at 2-MHz sample rate. This results in undersampling of the basic 5-MHz bandwidth signal. The picture begins to break up (loss of high-frequency components) with resulting high granularity and extensive edge business. Figure 8 is a sample of this encoding. The picture is of poor quality, but may be sufficient for the application.

1.3.5 3-Bit Encoded/Decoded DPCM (5 MHz)

The encoder/decoder was modified to operate at a 5-MHz sample rate (1/2 the Nyquist sample rate). The results of this undersampled signal are shown in Figure 9. The overall darkness in the picture is due to the photographic process. The picture is more than adequate for the intended application.

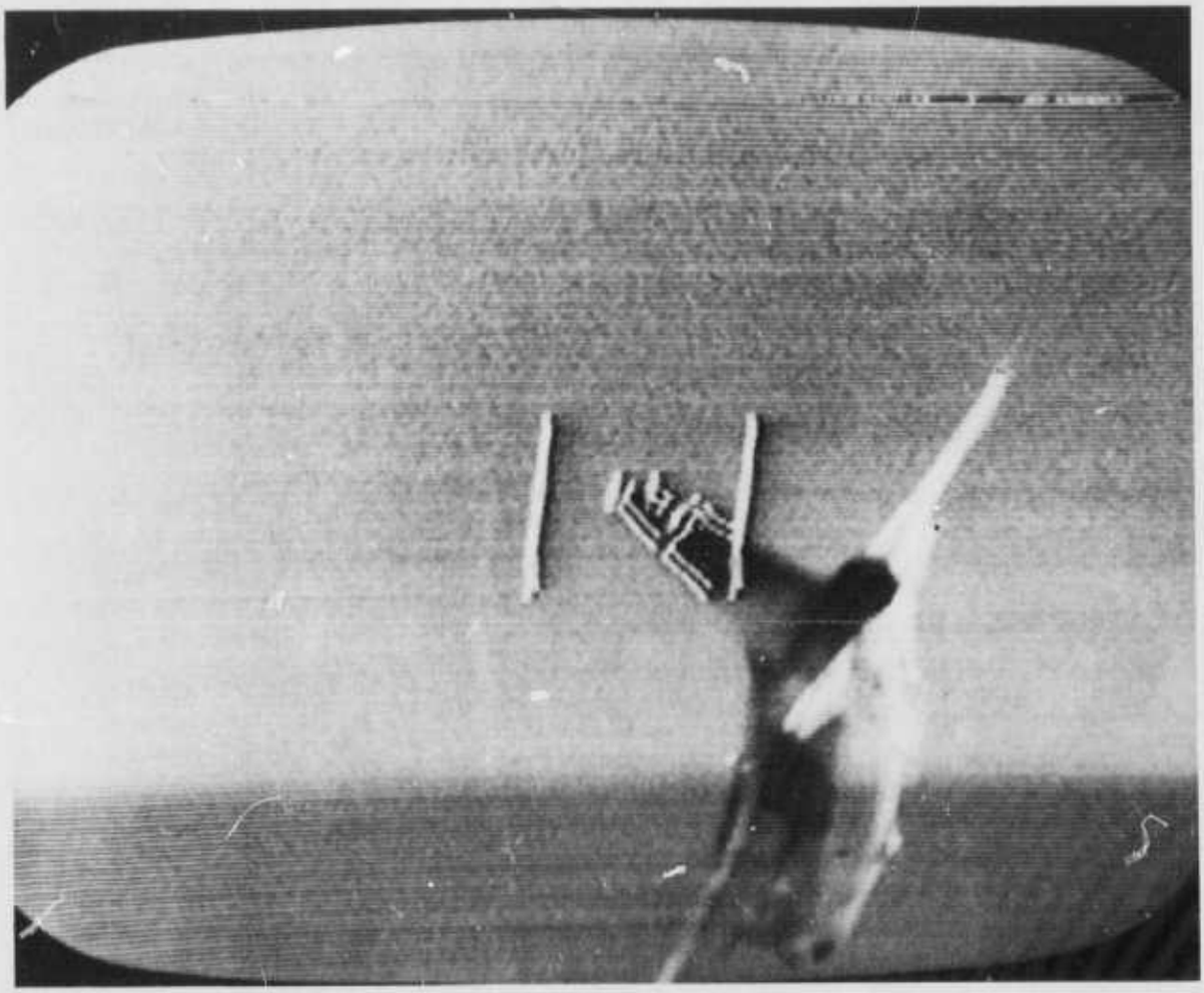

Figure 5. Typical Aircraft System Video Picture

Figure 6. 2-Bit Encoded/Decoded DPCM at 10 MHz

Figure 7. 3-Bit Encoded/Decoded DPCM at 10 MHz

Figure 8. 3-Bit Encoded/Decoded DPCM at 2 MHz

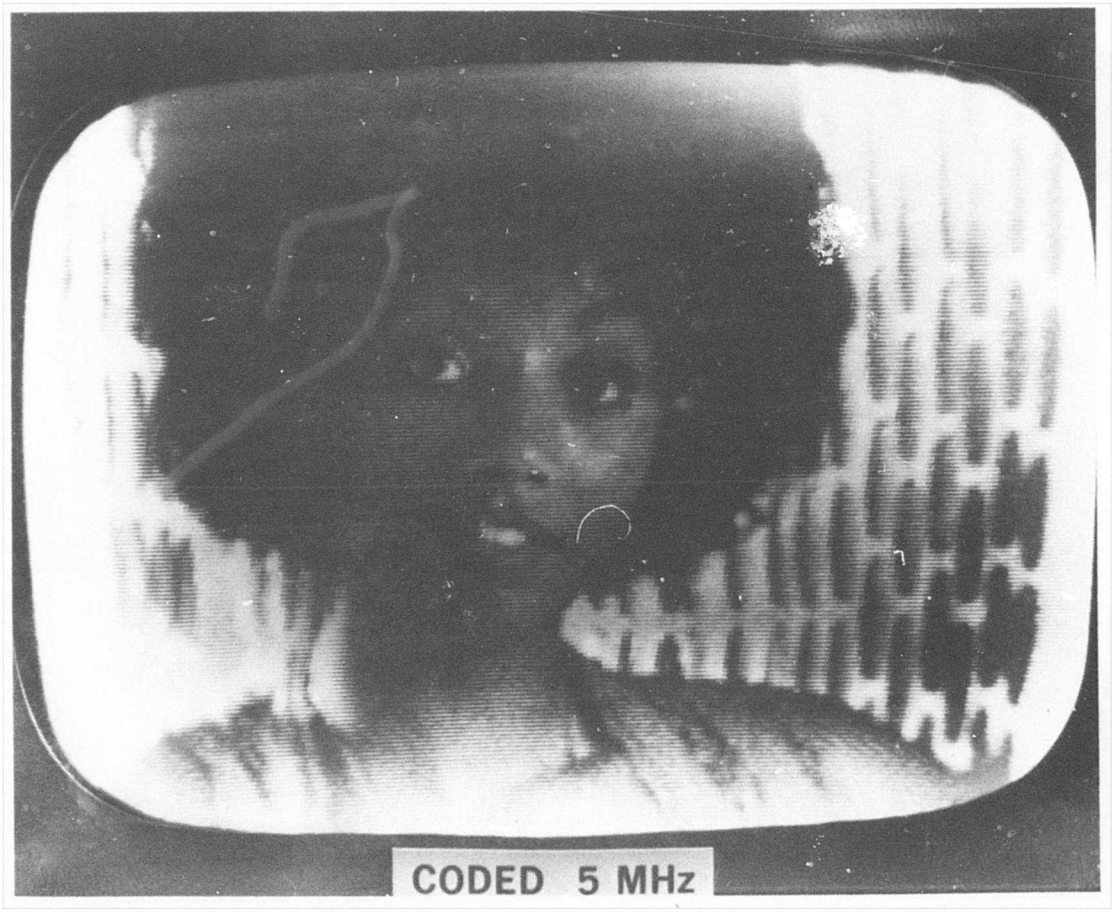

Figure 9. 3-Bit Encoded/Decoded DPCM at 5 MHz

1.3.6 3-Bit Encoded/Decoded DPCM (10 MHz)

Results of the encoder/decoder operating in normal mode 3-bit DPCM at a sample rate of 10 MHz (Nyquist sample frequency) is shown in Figure 10. The result is an excellent reproduction of the original photograph.

1.4 RESULTS

The effect of changing sampling frequency and number of bits per sample using the DPCM encoder/decoder is summarized in Table 1.

TABLE I. EFFECT OF CHANGING SAMPLING FREQUENCY AND BITS/SAMPLE

Figure No.	Sample Frequency, MHz	Bits/Sample	Bit Rate (MBPS)	Quality	Number of Video Pictures on a 100-Mbit/sec Link
3	Original	-	-	Reference	1
4	10 MHz	1	10	Sufficient	10
6	10 MHz	2	20	Good	5
7	10 MHz	3	30	Excellent	3
8	2 MHz	3	6	Poor	16
9	5 MHz	3	15	Good	6
10	10 MHz	3	30	Excellent	3

1.5 CONCLUSIONS AND RECOMMENDATIONS

1.5.1 Conclusions

The video encoder/decoder development program resulted in hardware that verified bandwidth compressions up to 16-to-1 can result in usable video pictures. These compressions can greatly enhance the distribution of video signals on either an aircraft or missile system by efficient use of available data channels through time division multiplexing.

Within the current state-of-the-art, the video encoder/decoder can be repackaged using large-scale integration to a usable hardware size for use in aircraft. Although logic speed and power dissipation were areas of concern in the breadboard, and will be in a flightworthy system, these items are controllable within today's environment.

Figure 10. 3-Bit Encoded/Decoded DPCM at 10 MHz

The data transmission system capable of bidirectional transmission at 200 MHz can be manufactured from today's hardware. Optical fibers, when suitable optical transmitters (LED's) are available, will provide additional advantages over the coaxial cable line. These advantages include:

- Weight and size reduction
- Reduction in signal quality degradation from external electromagnetic interference
- Minimize the electromagnetic interference caused by the link
- Reduced power consumption
- Higher data rates

1.5.2 Recommendations

To make the video encoder/decoder a viable bandwidth compression tool, an ongoing program will be required. This program should concentrate on the next logical stage of development--fabrication and test of a flyable prototype. The prototype should be developed to achieve the following goals:

(a) Minimum size

(b) Reduced Weight

(c) Low-power consumption

As a Phase II program, the first step would be an industry survey to determine size and weight of the unit. Specifications should be prepared and hardware estimates generated. Following these steps, procurement and fabrication of the hardware can occur. The existing breadboard provides a natural point of departure for development of the large-scale-integrated encoder/decoder. No further work on the bidirectional couplers and transmission system would be required in Phase II.

SECTION II

DESIGN APPROACH

Current production aircraft require large wire bundles to interconnect various components of the electronics systems on board. A solution to this problem is to multiplex these signals on to one cable. To investigate the feasibility of digitizing video signals to be included in these multiplexed cables, a video digital encoder/decoder has been developed and constructed that will encode, transmit, and reconstruct high-quality, real-time television pictures.

2.1 PROBLEM STATEMENT

The video output from a television camera is an analog voltage signal with blanking pulses inserted systematically to allow proper synchronization between television camera and monitor (Figure 11). The frequency bandwidth of the video signal depends upon camera quality and picture content. A video bandwidth of 5 MHz is specified for this encoder/decoder system. (Commercial television operates with a 4.5-MHz bandwidth.)

Digital sampling theory states that an analog signal must be sampled at a rate at least twice as high as the highest frequency component contained in the signal. This requires that the video signal be sampled at a minimum rate of 10 MHz (one sample every 100 nsec). Each of these samples or picture elements must then be assigned a digital code word that describes its amplitude. If 8 bits are assigned to the digital code word, the analog video samples may be quantized to 1 of 256 possible values. To transmit these data, a data rate of:

$$10 \times 10^6 \ \frac{\text{samples}}{\text{sec}} \times 8 \ \frac{\text{bits}}{\text{sample}} = 80 \times 10^6 \text{ bits/sec}$$

or 80 megabit/sec is required.

If this data rate requirement can be reduced without sacrificing picture quality, then more video channels may be multiplexed onto a given data bus, or alternately, a single video channel could be transmitted on a less sophisticated data bus.

2.2 SOLUTION

Since a typical television picture contains a significant amount of redundant information and the ultimate viewer has physiological limitations and subjective preferences, there are many potential image coding methods that can be used to achieve the goal of data rate reduction. (These are described in Appendix A).

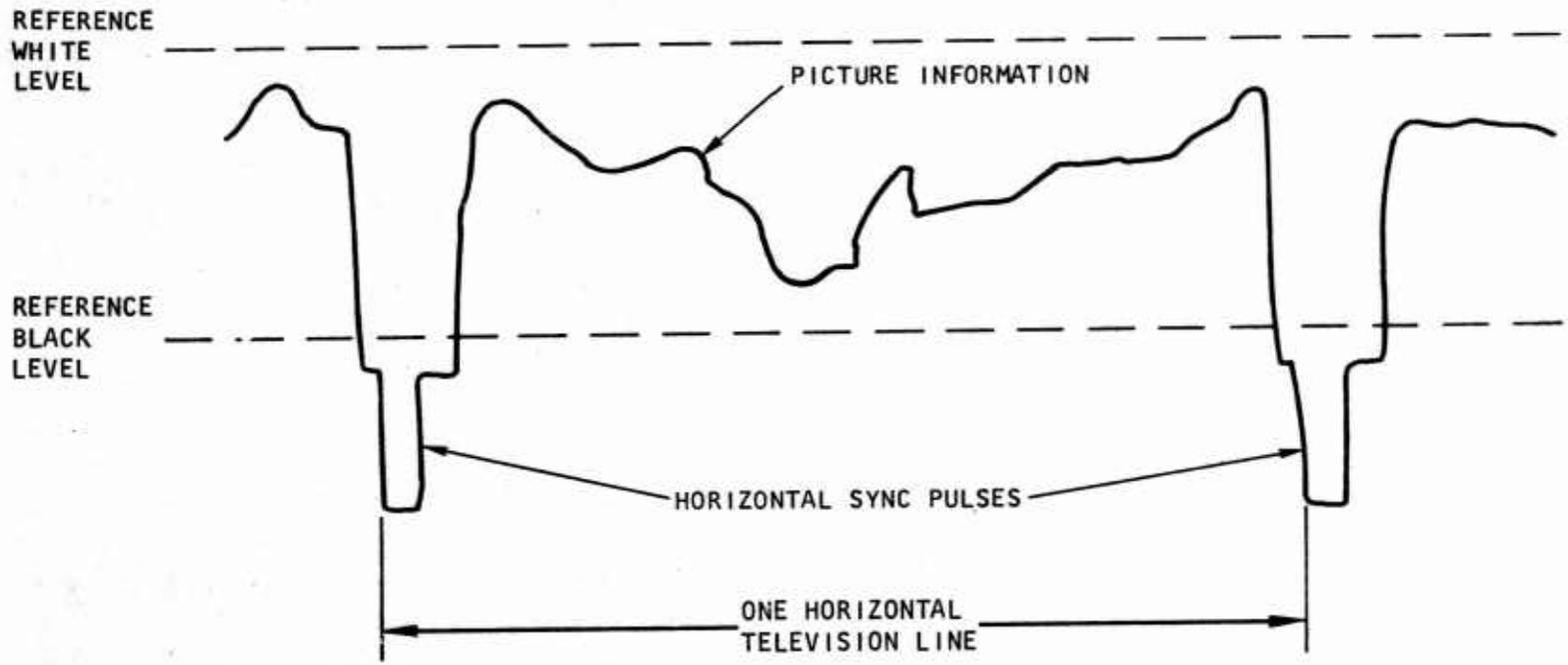

Figure 11. Typical Video Waveform

Studies conducted during the initial phases of this contract compared the various available coding methods based on:

- The amount of data reduction provided
- The quality of the reconstructed television picture
- The requirement to remain within the current state-of-the-art of available electronic circuits
- The ease of fabrication and miniaturization of the final hardware

The optimum coding technique resulting from these studies is differential pulse code modulation (DPCM) coding.

DPCM coders compare the present sample picture element with the preceding sample picture element, and only the difference is digitally encoded and transmitted. Since the difference signal is much smaller than either picture sample, fewer bits can be used to adequately describe it. The small digital difference signals are accumulated in a feedback element and the output of this accumulator constantly tracks the video input signal due to the servomechanism action of a feedback loop in the coder. To reconstruct the video signal at a receiver, the digital difference signal is accumulated in a duplicate feedback element. The output of this second accumulator also tracks the original video input signal. A simplified block diagram of a DPCM encoder and decoder is shown in Figure 12.

2.3 CIRCUIT DESIGN STRATEGY

The parameter of primary importance in implementing the DPCM coder is the time allowed between samples of the video signal. This system samples the video input at the minimum Nyquist rate of 10 MHz, which allows 100 nsec to perform the following functions:

(a) Sample the difference signal

(b) Quantize and convert to a digital code word

(c) Add this code word to the result stored in the accumulator

(d) Output the accumulator for comparison with the input video signal

(e) Make the comparison and allow the new difference signal to become stable

Candidate circuit implementations that were examined revealed that the settling times associated with discrete analog devices (e.g., summing amplifiers, sample-and-hold modules, etc.) would consume an inordinate portion of the loop time available to perform the coding functions. As a result, a primarily digital circuit implementation was designed. Important consequences of this circuit design strategy are:

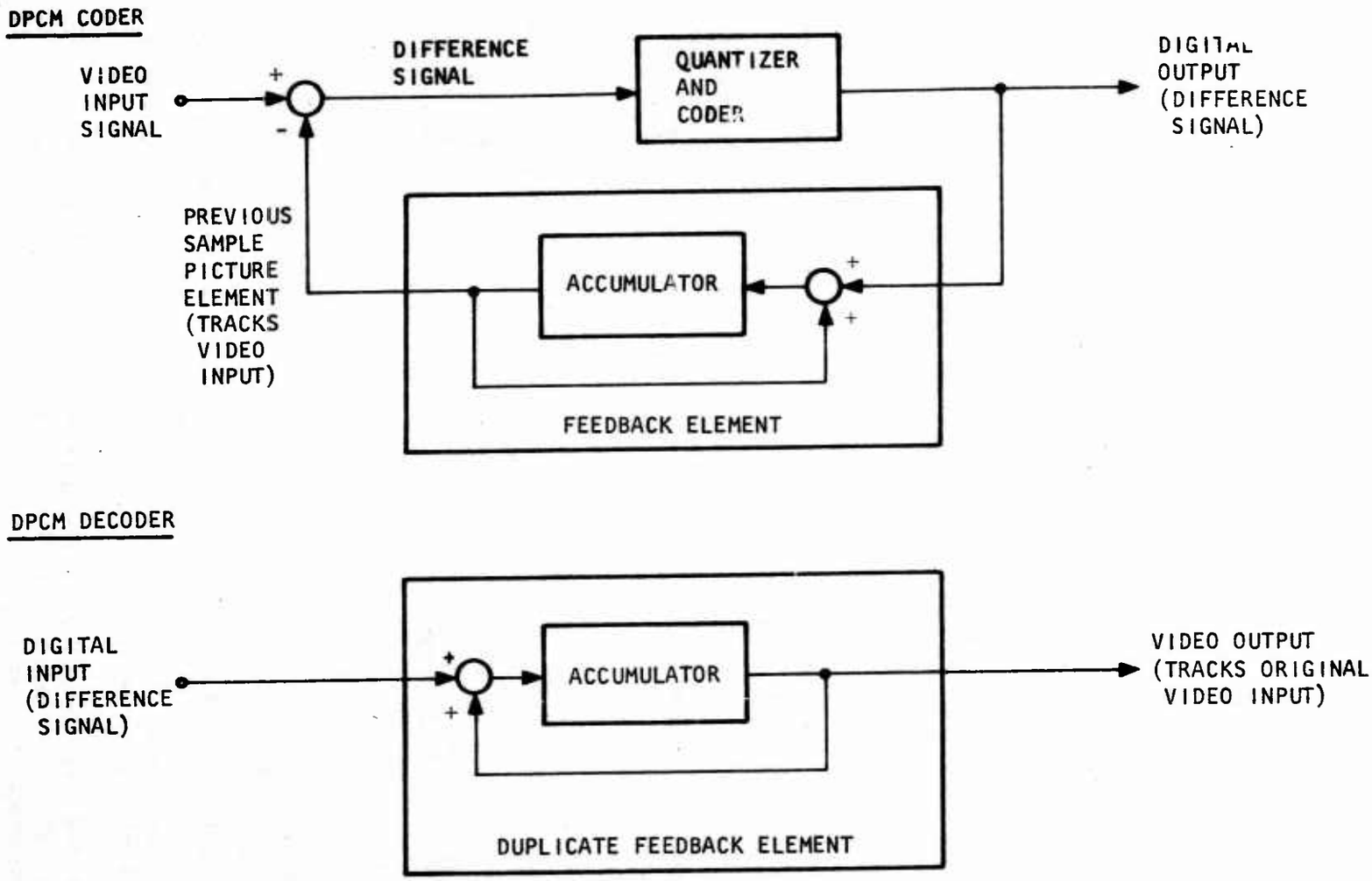

Figure 12. Simplified Block Diagram

(a) Circuit components could be selected from among a limited number of well-established integrated circuits readily available from multiple sources.

(b) The accumulators in the coder and decoder could be implemented with a digital adder circuit and a storage register, thus eliminating the precision components associated with analog integrators.

(c) The digital accumulators would ensure perfect tracking between the DPCM coder and decoder because the circuits are identical.

(d) Lengthy calibration procedures associated with analog offsets, leakages, and drift would be eliminated.

(e) The standard building blocks of a digital device family readily lend themselves to large scale integration (LSI), in which many devices are combined onto one large integrated circuit, thus drastically reducing size, weight, and power consumption.

2.4 COMPONENT SELECTION STRATEGY

To perform the DPCM coding within the allotted 100-nsec loop time, a logic family is required that has propagation delays of only a few nanoseconds. There are two logic families widely available that have the required speed capability: (1) high-speed Schottky TTL, which is a saturating logic family, and (2) the non-saturating emitter-coupled-logic (ECL) family. Both families are widely available from multiple sources and have a wide variety of functional elements. Gate propagation delays for the ECL family range from 1.0 to 3.0 nsec, while the Schottky TTL ranges from 3.0 to 5.0 nsec.

The emitter-coupled-logic family produced by Motorola Semiconductor Products, known as MECL, was selected for this prototype feasibility application. More detailed information leading to this selection is presented in Appendix B. The MECL I family was the first digital monolithic integrated circuit line produced by Motorola and was introduced in 1962. The higher-speed versions--MECL III and MECL 10,000--used in this unit were introduced in 1968 and 1971. The rationale for selecting the MECL logic family over the Schottky TTL for this application are as follows:

(a) The MECL line is 1.5 to 2.0 times faster than the Schottky TTL line, allowing more time margin for the remaining analog sections of the coder loop.

(b) The ability of MECL logic to drive transmission lines allows longer signal paths. This is important in the fabrication of a prototype breadboard where ultimate packing density is a hindrance to system changes and evaluation.

(c) The non-saturating MECL family generates less noise than the saturating TTL logic, which is important in an uncontrolled breadboard environment.

(d) The level comparators used to quantize the small analog error signals have an ECL output stage that can directly interface with MECL coder logic, thus increasing system speed.

(e) MECL circuits have complementary outputs and can be "wired-or" connected, again increasing system speed and also reducing package count.

(f) MECL circuitry draws relatively constant power without the switching spikes associated with all TTL circuitry. This allows program time and money to be concentrated on the coder design rather than expended on the acquisition of high-quality power supplies.

SECTION III

THEORY OF OPERATION

To demonstrate the feasibility of digitizing television signals and to investigate the quality of these digitized pictures, a system utilizing a DPCM encoder and decoder was constructed. A block diagram of the complete encoder/decoder system is shown in Figure 13. The purpose and function of each of these blocks are discussed below.

3.1 VIDEO SIGNAL CONDITIONER

The video signal conditioner buffers the incoming video signal and provides the proper input impedance to match the video source. The video signal is ac-coupled into the coder system and then clamped to a reference dc level to provide stable operating voltage ranges within the coder system. The video signal is then low-pass-filtered to eliminate spurious signal components above 5 MHz, which would cause aliasing errors due to the sampling nature of the coder. The video sync pulses are detected and output for use in coder reset and error correcting circuitry described in paragraph 3.4.

3.2 3-BIT DPCM ENCODER

The conditioned video signal is compared with the encoder feedback signal (which represents the previous video sample picture element), and an analog difference signal is formed. The difference signal is quantized to determine its voltage level (one of eight ranges, with four positive and four negative). The voltage level ranges have a nonlinear characteristic to optimize coder performance. Small difference signals are detected in a narrow band centered around zero volts to provide good coder performance during slowly changing portions of the television picture. Large difference signals are detected in progressively increasing voltage ranges to allow the coder to track fast changing edges of the television picture.

The output of the quantizer is assigned a digital code word by the coder. Three bits are sufficient to describe the eight possible levels of difference signal generated by the level detectors of the quantizer. The digital code word is output from the encoder by the line-driving circuitry of the output buffer register. The digital output code words also are provided in a suitable format (sign plus magnitude) to the digital adder in the DPCM encoder feedback loop. The digital adder circuitry adds or subtracts the digitized difference signal to the previous picture sample, which is stored in the 8-bit accumulator storage register, generating a new picture sample that is restored in the accumulator storage register. This new picture sample is converted back into an analog voltage by the D/A converter. The output of the D/A converter is then ready to be compared against the video input signal to generate the next difference signal.

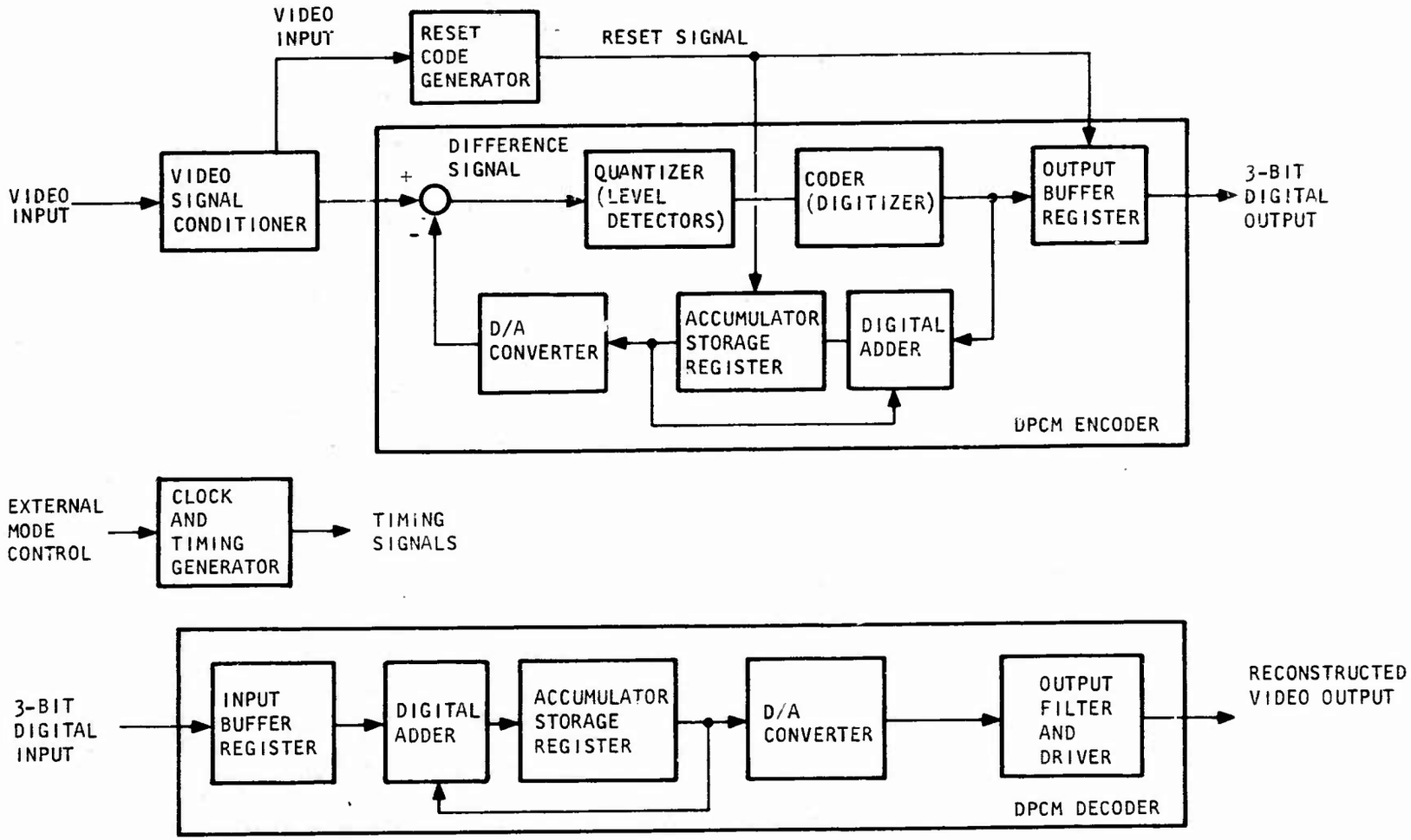

Figure 13. System Block Diagram Video Encoder/Decoder

The DPCM encoder steps along as described above and generates samples of the input video signal every 100 nsec. The feedback element of the DPCM encoder provides a servomechanism action that forces the output of the D/A converter to track the input video signal. A duplicate feedback element in a receiver DPCM decoder also tracks the input video signal.

3.3 3-BIT DPCM DECODER

As stated above, the DPCM decoder is implemented as the duplicate of the feedback element utilized in the DPCM encoder section. The 3-bit digital signal transmitted by the encoder is received in an input buffer register. The output of the buffer register is changed to sign-plus-magnitude digital format. The adder circuitry adds or subtracts this digital difference signal to the contents of the accumulator storage register so that the accumulator contents can track the input video signal identical to the encoder accumulator. The content of the accumulator storage register is converted back to an analog video signal by the D/A converter. The output of the D/A converter is filtered to smooth the piecewise linear D/A waveform, and an output driver amplifier is used to ac-couple the reconstructed video waveform out of the system and to match the impedance of the video monitor used to view the television pictures.

3.4 RESET CODE GENERATOR

The function of the reset code generator is to correct the error effects that might possibly acrue due to random circuit malfunctions or digital transmission errors occurring between the encoder (transmitter) and decoder (receiver) sections of the system. Since the digital signal transmitted represents successive difference signals, it is important that both the encoder and decoder sections maintain an absolute reference level so that the difference signals will accumulate relative to a stable base value. The digital implementation of the system provides a simple method to achieve this error correction function.

The video input signal contains sync pulses occurring once every horizontal line of the television picture. The tips of the sync pulses are the most negative value of the input video waveform, and during these sync pulses the television picture is blacked out to allow the cathode ray of the picture monitor to fly back across the screen to begin a new horizontal television line.

Since the video tips represent the most negative signal value achieved, it is convenient to represent this signal value with all 0's in the accumulator storage register (that is; a completely depleted accumulator). This provides two benefits: (1) it allows the maximum use of the dynamic range of the accumulator, and (2) it provides the necessary drift-free, absolute reference level. Since there is no picture information during the sync pulse period and the accumulator contains all 0's during the sync pulse period, the sync pulses are detected by the video signal conditioner, and the reset code generator uses this information to override the encoder accumulator register and force the contents to the all-0 state.

Resetting the encoder accumulator ensures that the DPCM encoder loop is automatically realigned at the beginning of each horizontal television line, but it is also necessary to ensure that the DPCM decoder accumulator is reset simultaneously. To achieve this, the reset code generator simply overrides the contents of the encoder output buffer register and causes an output code word to be transmitted that represents a maximum, negative difference signal. This code word is transmitted for enough output periods to ensure that the DPCM decoder accumulator register is completely depleted. The decoder accumulator now matches the encoder accumulator, and when the reset code generator output stops, both accumulators are released and continue to track together.

In the event that the reset code generator fails to receive a sync signal from the video signal conditioner, it contains a free running counter that is allowed to run and generate an independent reset signal.

3.5 CLOCK AND TIMING GENERATOR

The function of the clock and timing generator is to provide the proper timing signals to sample the video signal and update the digital logic circuitry of the encoder/decoder system. The clock is normally derived from a 60-MHz crystal-controlled oscillator contained within the system and counted down by the timing generator to achieve the 10-MHz sampling rate. An external oscillator is provided so that the system can be operated at sampling rates other than 10 MHz. The system clock and timing generator also can be run in a single step mode to facilitate system setup and troubleshooting procedures.

SECTION IV

BREADBOARD SYSTEM FABRICATION

To verify the predicted performance of the DPCM television coder and the validity of the circuit design implementation, a breadboard prototype system was constructed and operated. The breadboard is self-contained, portable, and can be operated with either 60- or 400-Hz, 115-vac power. The video encoder/decoder breadboard and power supply unit are shown in Figure 14.

4.1 PACKAGING CONCEPT

Breadboard system configuration and packaging was evolved to meet the following requirements:

- Easy to build and modify
- Simple to use
- Easy to test and evaluate
- Provide proper electrical environment for the wide bandwidth video signals and the nanosecond edge speeds of the digital logic.

The video input to the system and the reconstructed video output from the system are at readily identified BNC-type connectors on the front panel. Switches are provided to allow selection of the system timing mode. Operation can be from the internally available clock source or from an externally applied clock source. Single step clock operation also is provided. The front panel contains light emitting diode (LED) displays that indicate the contents and overflow conditions of both the encoder and decoder accumulator storage (adder) registers, the 3-bit DPCM line code transmitted between encoder and decoder sections of the system, and the sign plus magnitude code representing the encoder difference (error) signal. Switches are provided to override the contents of both the encoder and decoder accumulator storage registers. Timing signals are provided as outputs at BNC-type connectors to serve as trigger waveforms for external test equipment. A closeup view of the front panel controls is shown in Figure 15.

Conversion of the available ac power source to the dc power required by the encoder/decoder breadboard is accomplished using commercially available open-frame power supplies mounted on a separate chassis. Power is supplied to the breadboard through an interconnecting power cable to a multi-pin connector at the rear of the breadboard unit.

The internal construction of the breadboard (Figure 16) was designed to provide simple access to all circuitry. The top cover of the breadboard slides to the rear, exposing the inside of the unit. All circuitry is on four

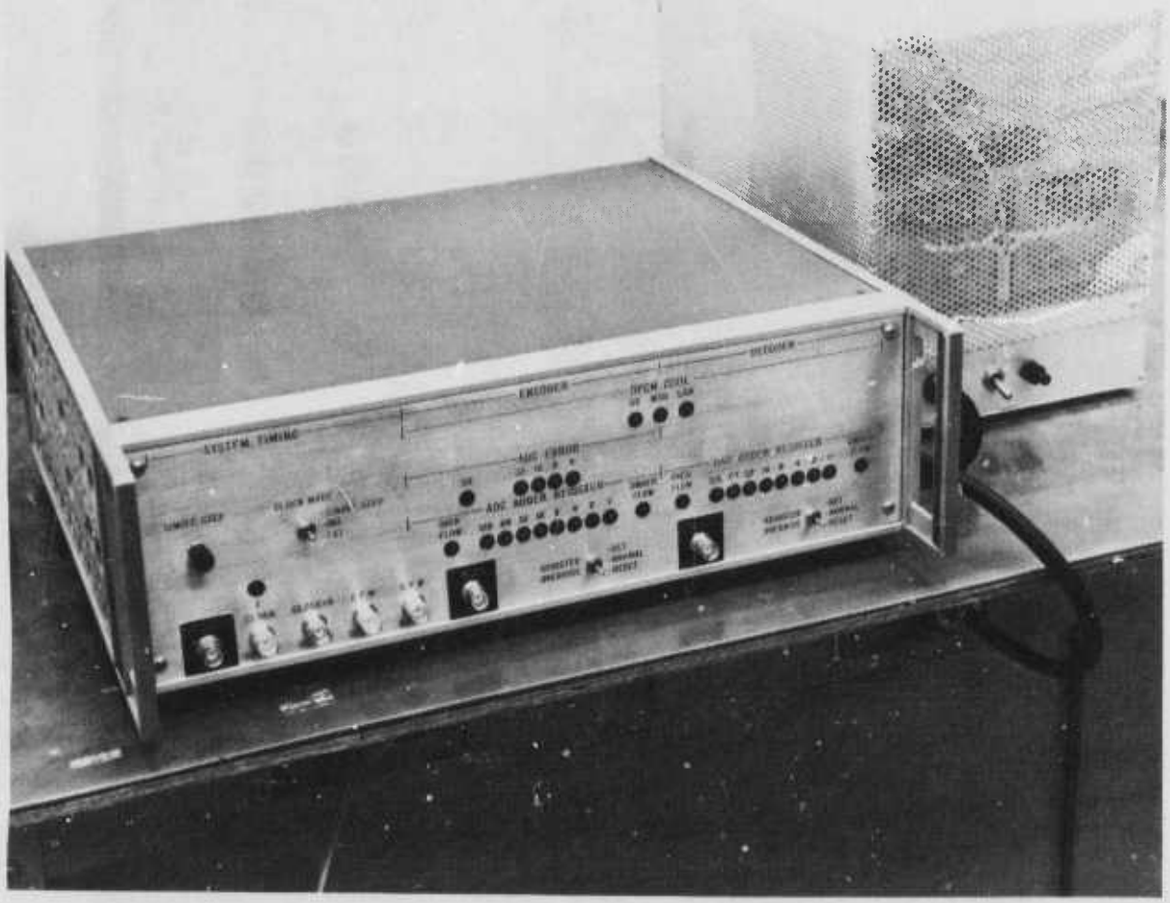

Figure 14. Video Encoder/Decoder Breadboard and Power Supply Unit

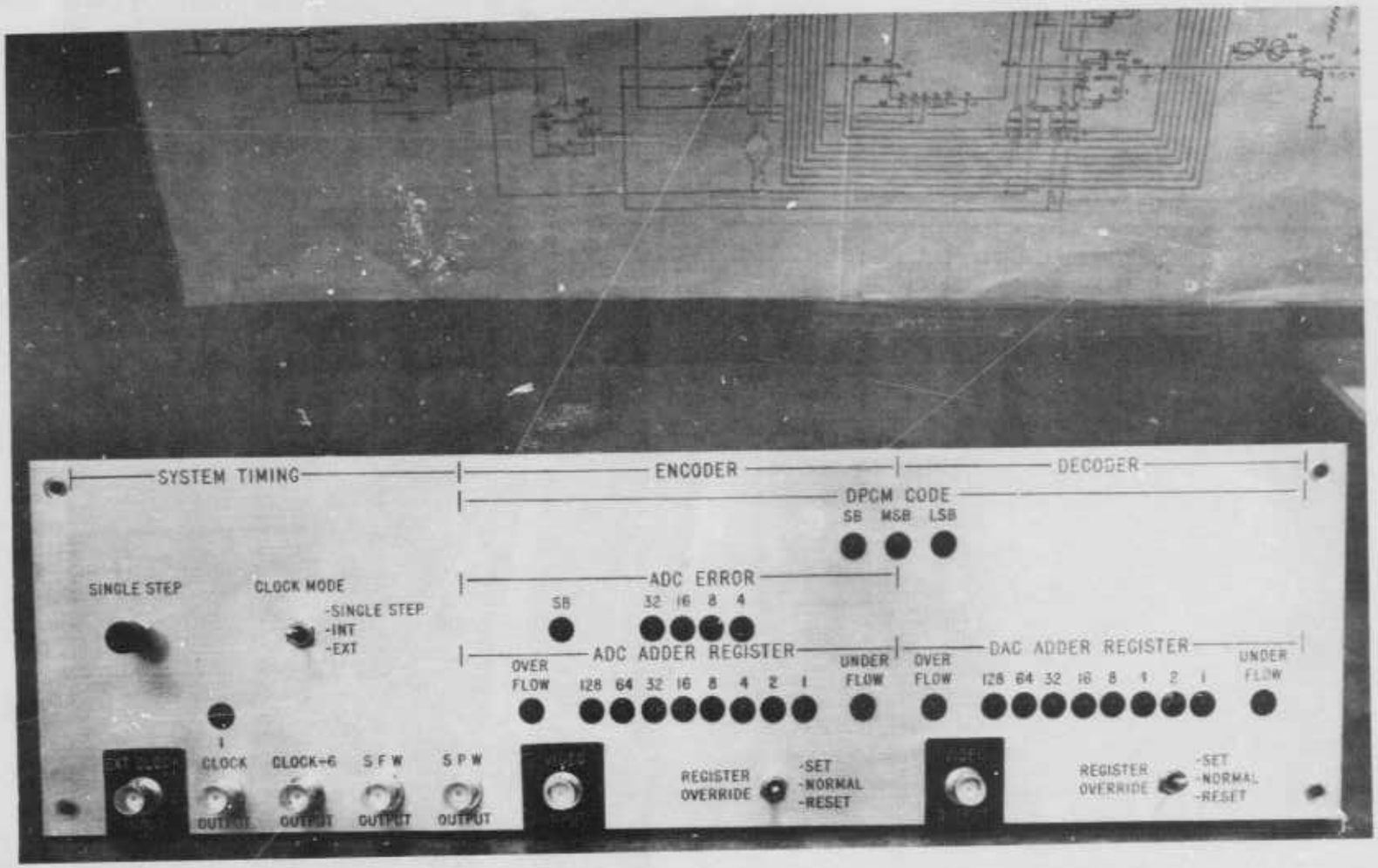

Figure 15. Breadboard Front Panel Controls and Displays

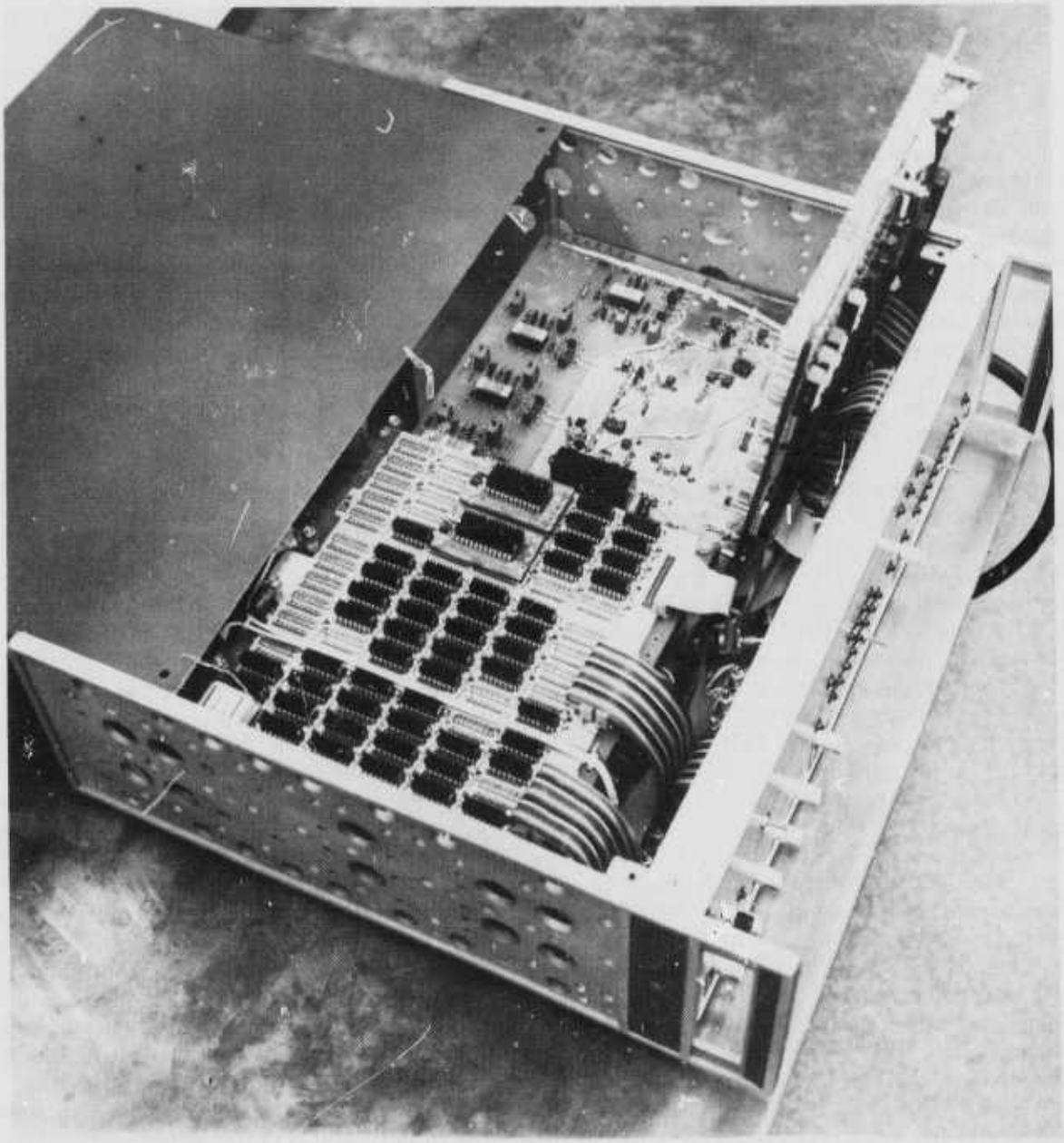

Figure 16. Internal Construction of Video Encoder/Decoder Breadboard

boards: two horizontal analog circuit boards at the bottom of the breadboard chassis and two digital logic boards mounted directly above the analog circuit boards. Interconnections between boards utilize flexible flat ribbon cable. Interconnections to the breadboard front panel also use flexible flat ribbon cable, except for the video input and output signals that are carried on microdot miniature coax cable. The digital logic boards are mounted on hinged posts so that they can be pivoted up to expose the analog circuit boards underneath. Signals and waveforms at every component in the system can be monitored during system operation, facilitating system investigation, checkout, and troubleshooting.

4.2 CIRCUIT PARTITIONING

The primary concern during partitioning of the breadboard circuitry was to minimize the length of signal wires between components, thus minimizing propagation delays and the effects of stray wiring capacitance and inductance that cause impedance mismatches and undesirable ringing on circuit waveforms. The breadboard was partitioned into two sections: a transmitter section containing the video signal conditioner, DPCM encoder, and reset code generator; and a receiver section containing the DPCM decoder and the system timing generator. Each section contains two boards, one for the digital integrated circuits and one for the corresponding analog circuitry for that section. Circuit component layout on the boards is arranged to produce minimum signal flow paths from board input to output and between critical circuit elements.

The boards for the digital logic are controlled impedance logic panels specifically designed for emitter-coupled-logic integrated circuits (IC's) in 16-pin, dual-in-line packages (DIP's.) The logic panels are produced commercially by Augat, Inc. The boards contain a power voltage plane on one side and a ground plane on the other. Both planes are bussed to the appropriate pins at each IC socket location, establishing a low-impedance power distribution on the board. A third internal voltage plane is available at each socket location for use as a termination voltage as required. Signal interconnections are made using standard wire wrap on the back side of the board. All IC's are plugged directly into the logic board except for the 24-pin dip package of the MC10181 arithmetic logic units (adders) and the crystal controlled clock. These devices are plugged into small adapter boards that are plugged directly into the logic board.

Since the breadboard is designed for easy access to all components, the boards are not constrained by chassis-mounted edge guides which would also function to remove component heat. Instead, individual finned heat sinks are epoxied to each IC package and heat is removed by convection. Since the heat sinks cover the component part identification marking, a large code letter is at the end of each heat sink to identify the fifteen different digital IC's used in the breadboard. The top and bottom sides of the two Augat boards used in the breadboard are shown in Figures 17 through 20. Augat board No. 1 contains the digital logic for the DPCM encoder and reset code generator. Augat board No. 2 contains the digital logic for the DPCM decoder and the clock and timing generator.

The boards for the analog circuitry of the breadboard are made using epoxy glass circuit boards produced commercially by Circuit-Stik, Inc. These boards

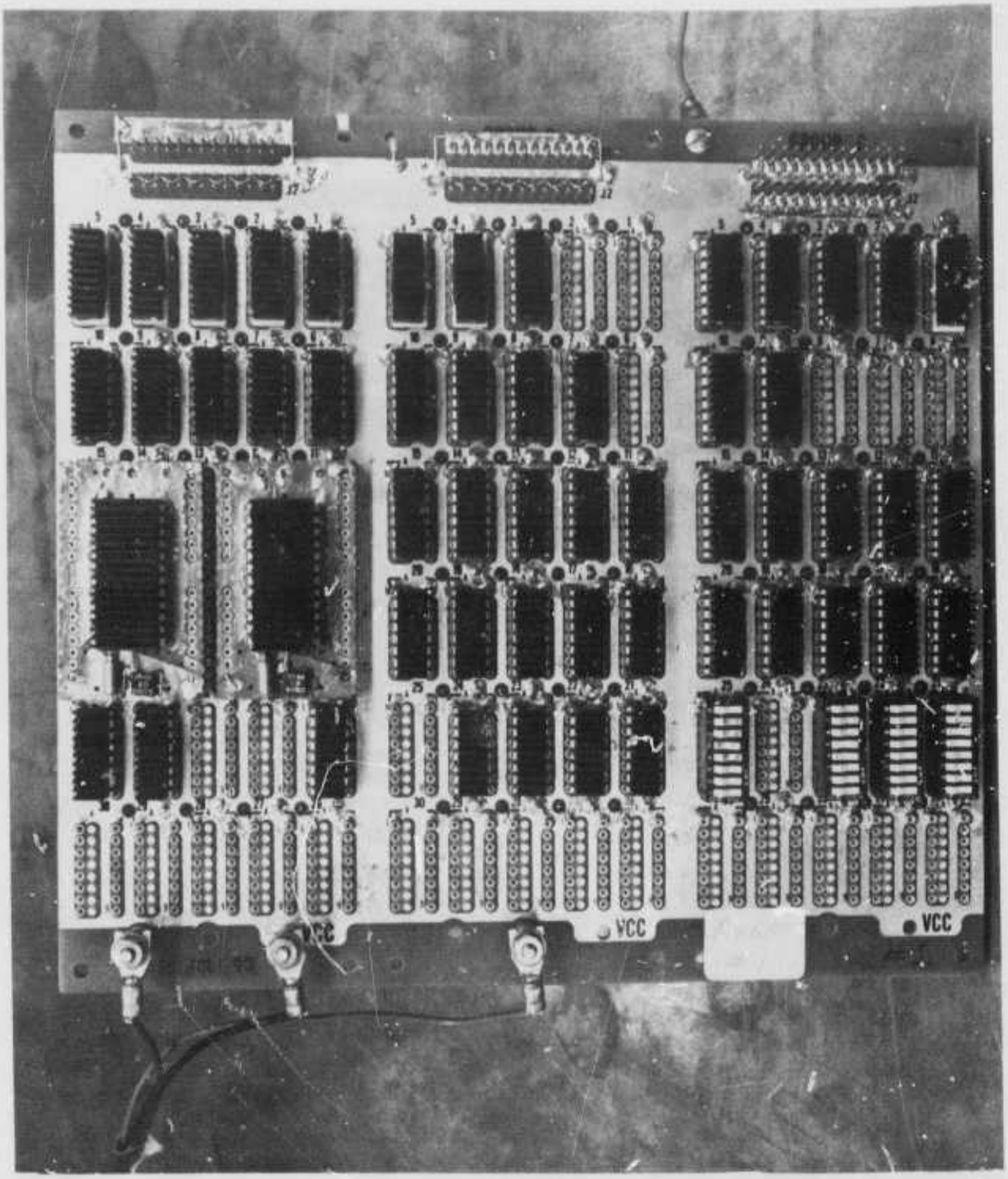

Figure 17. Top View, Augat Board Number 1

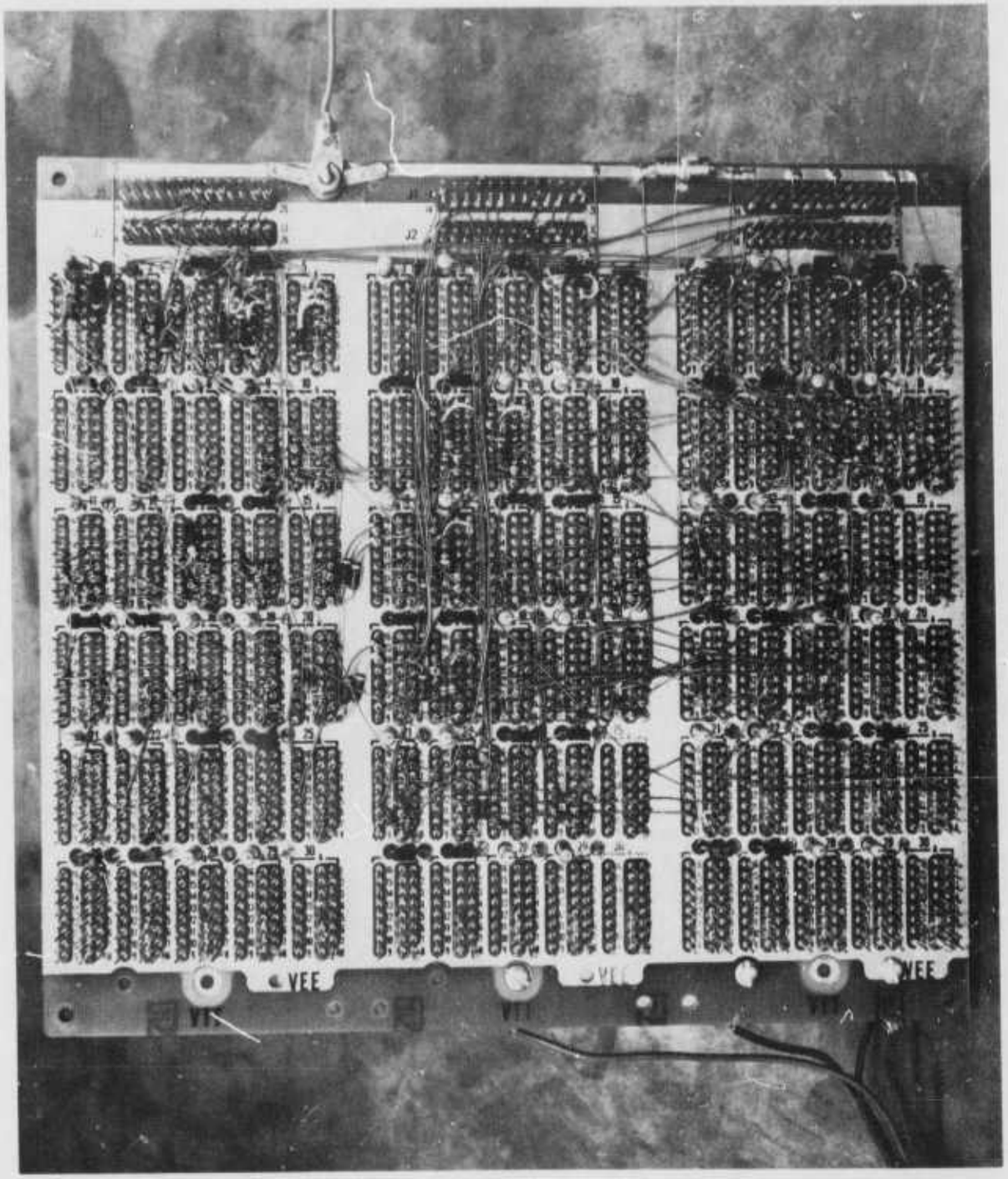

Figure 18. Bottom View, Augat Board Number 1

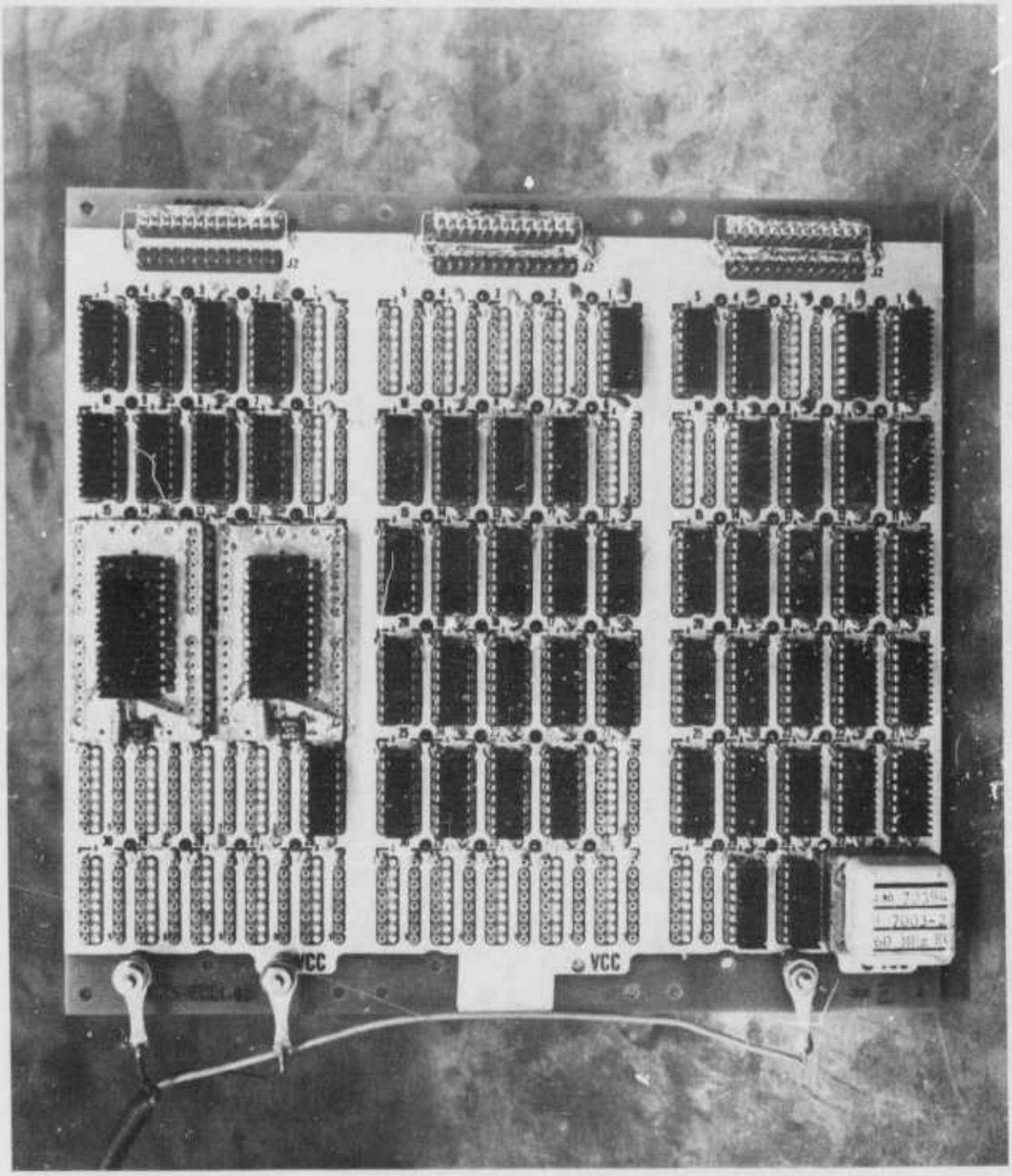

Figure 19. Top View, Augat Board Number 2

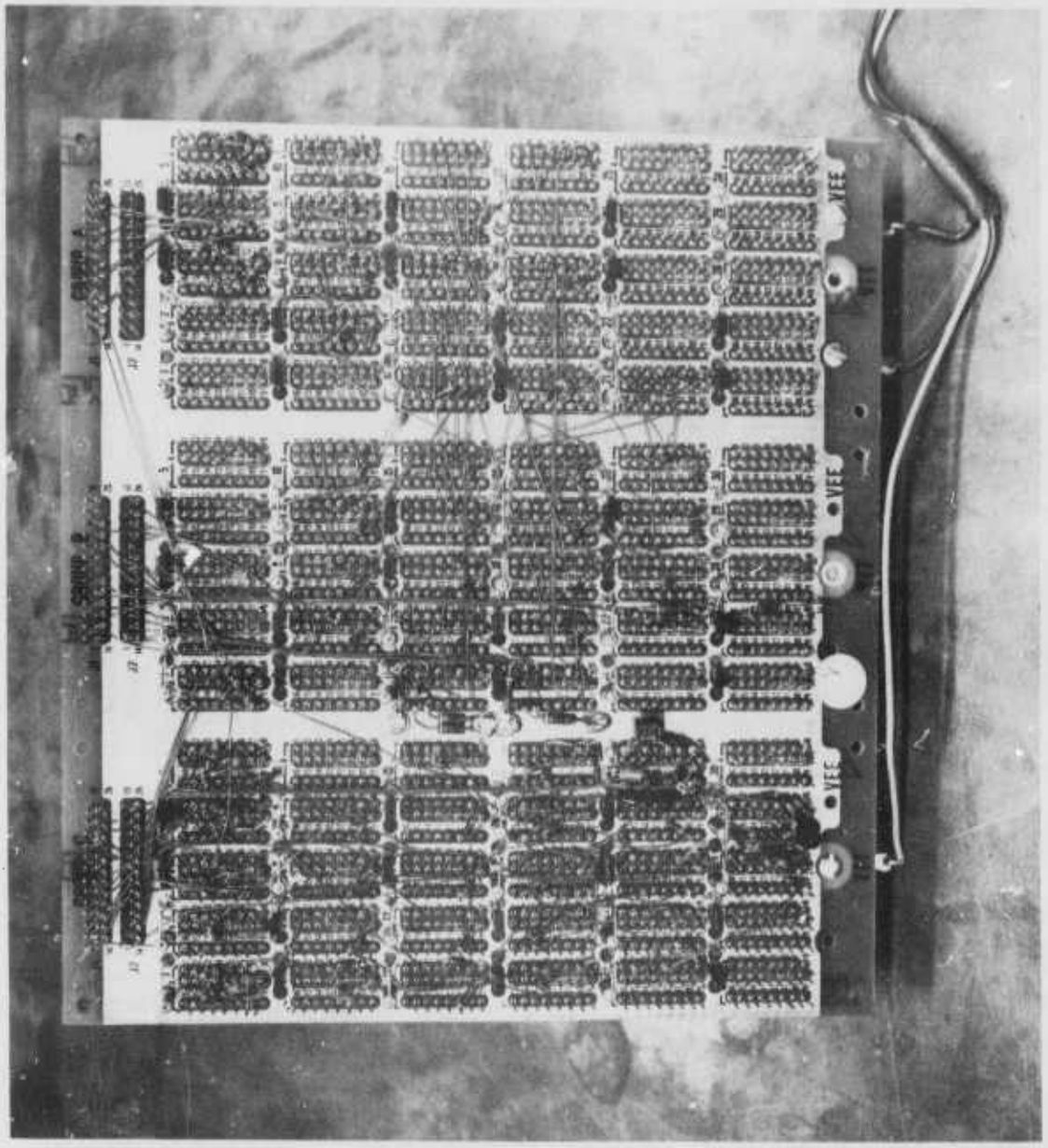

Figure 20. Bottom View, Augat Board Number 2

have precision-drilled, 0.042-in.-dia holes on a 0.100-in. grid pattern. The boards are covered on both sides with copper foil. Circuit patterns are drawn onto the copper foil, which is then cut and peeled. Large areas of the copper foil on the boards serve as a ground plane for the circuitry. Sockets are installed on the boards to facilitate IC installation and removal. Discrete resistors and capacitors are soldered directly to swaged-in terminals, and signal interconnections are made by the component leads or hardwire. Power is distributed on the board using Stripline conductors (also available from Circuit-Stik, Inc.). These conductors use a flat conductive strip with an insulating backing and are simply pressed into place on the board.

The top and bottom sides of the two analog circuit boards are shown in Figures 21 through 24. Analog circuit board No. 1 contains the video signal conditioner, the 5-MHz filter, error signal summing amplifier, D/A converter, and level detector reference generator used in the DPCM encoder section of the breadboard. Analog board No. 2 contains the D/A converter and output filter-buffer amplifier used in the DPCM decoder section of the breadboard.

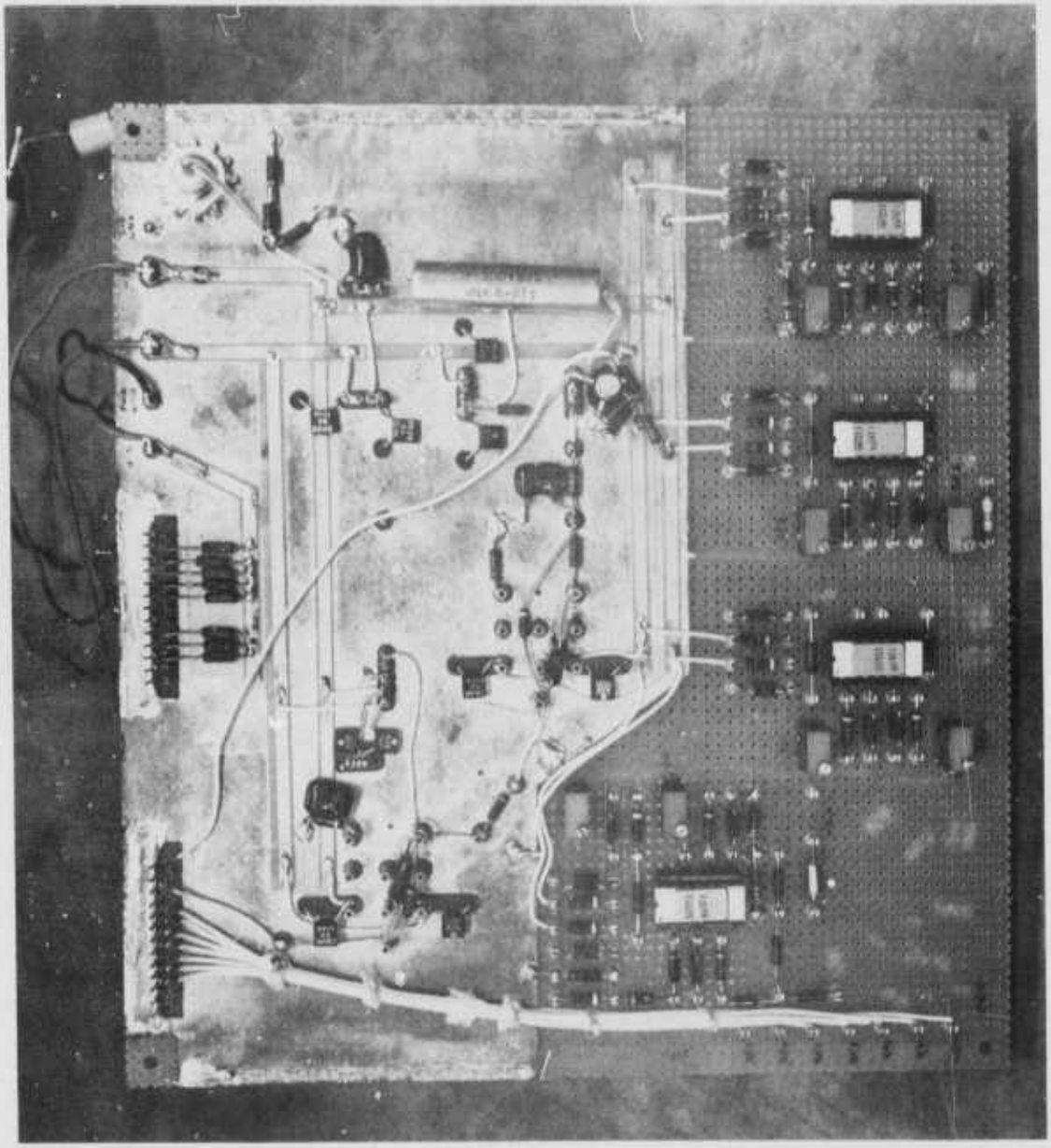

Figure 21. Top View, Analog Circuit Board Number 1

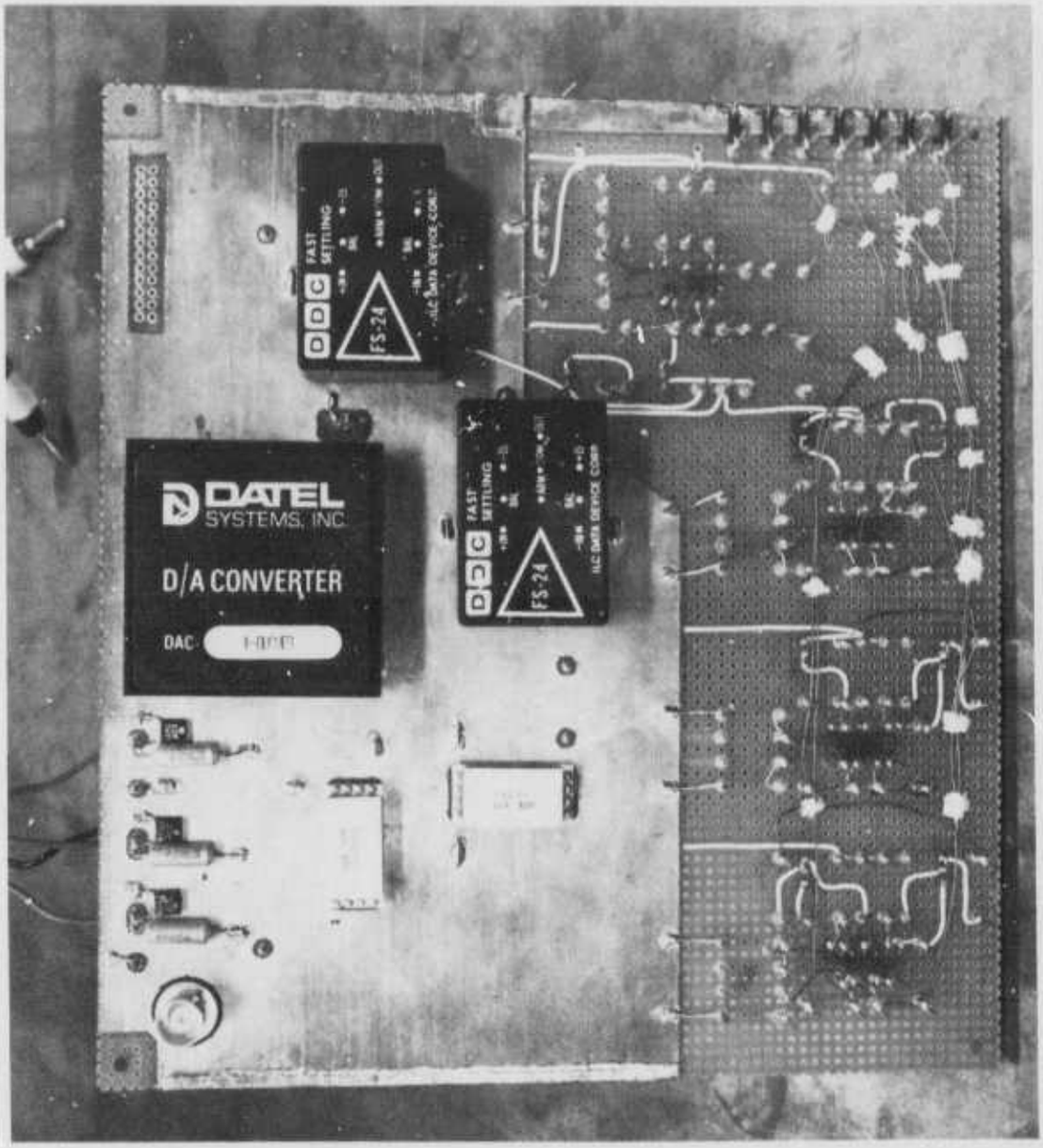

Figure 22. Bottom View, Analog Circuit Board Number 1

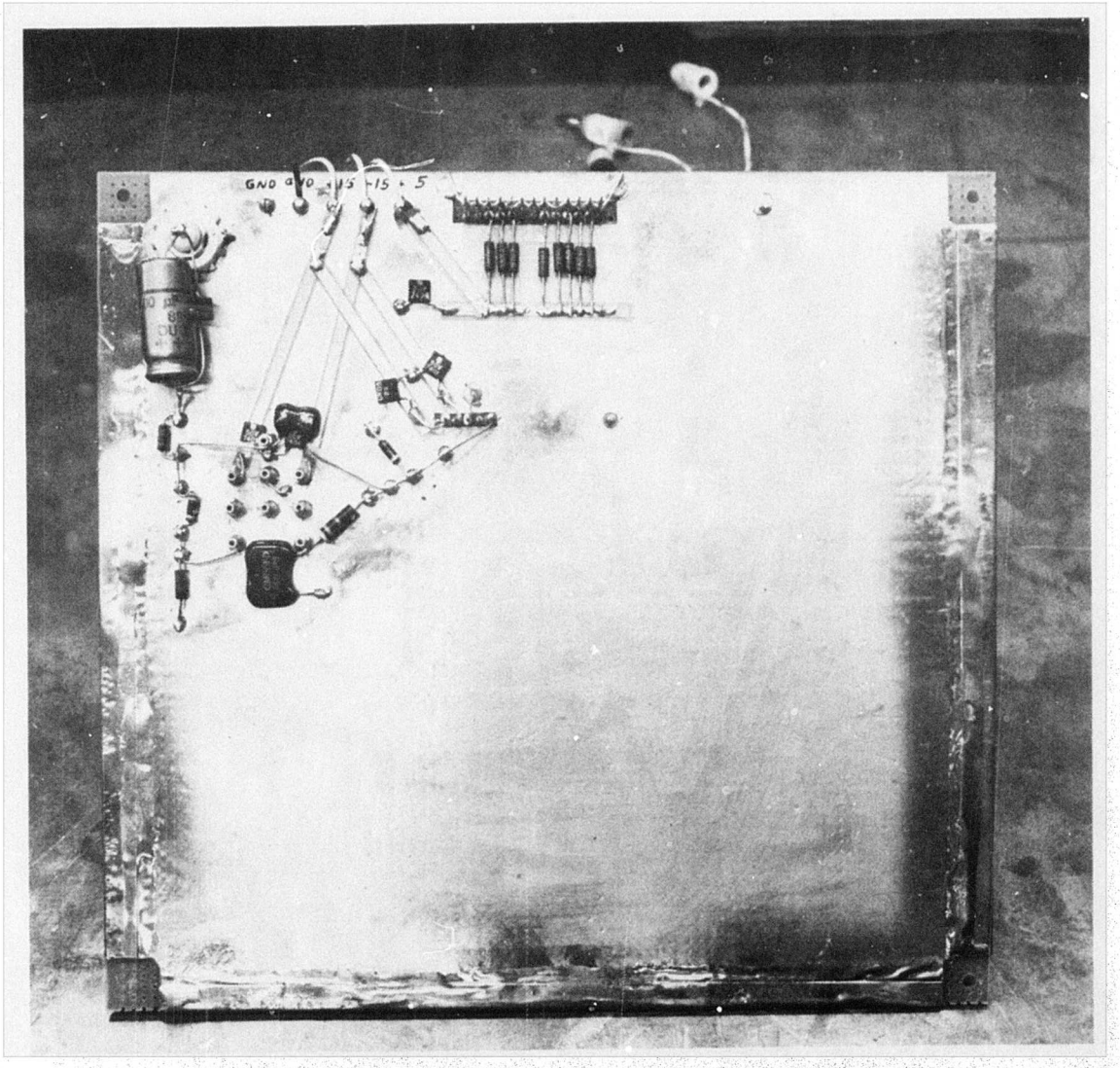

Figure 23. Top View, Analog Circuit Board Number 2

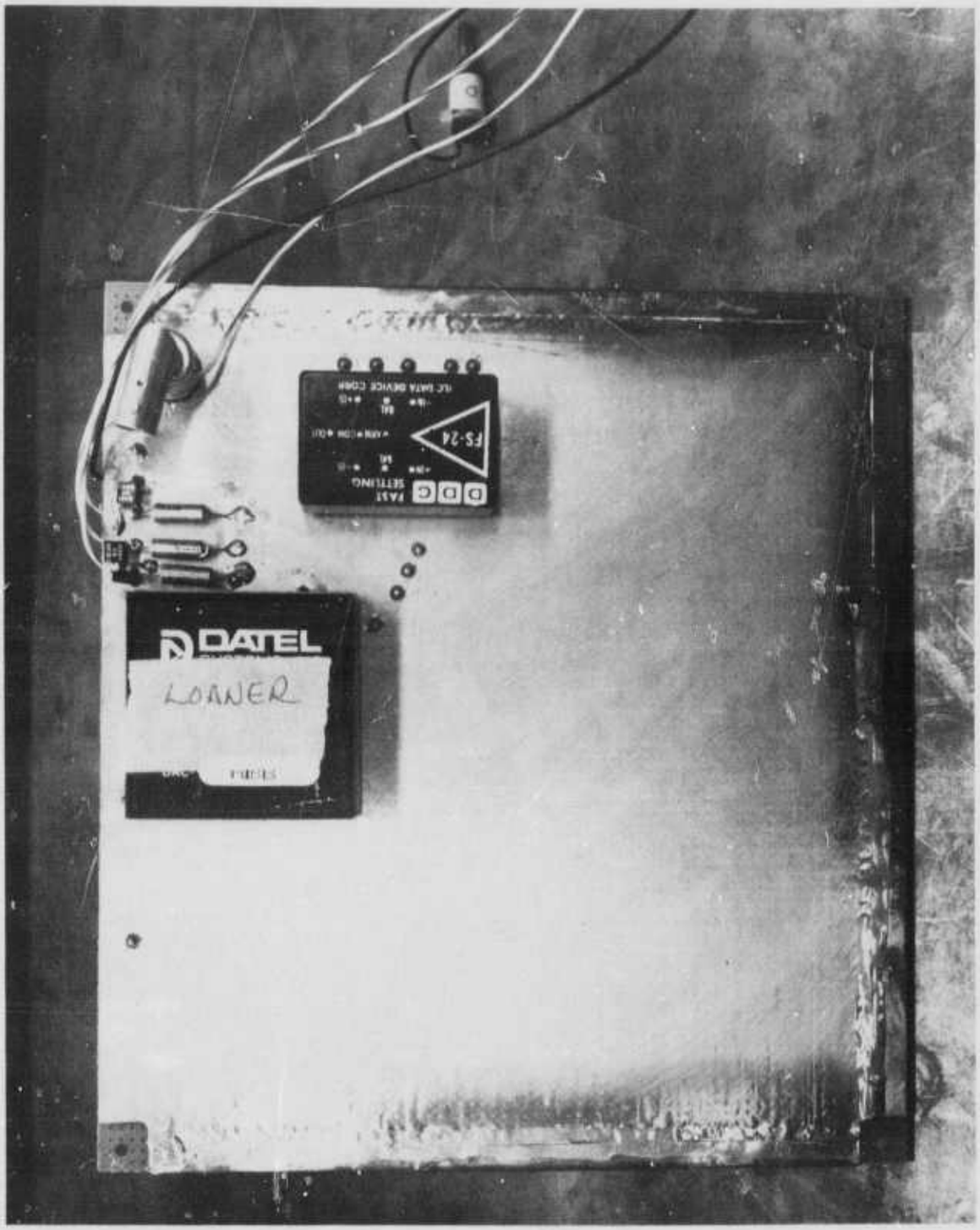

Figure 24. Bottom View, Analog Circuit Board Number 2

SECTION V

PROGRAM RESULTS

To investigate the feasibility of digitizing video signals for inclusion in a digital data multiplexing system, a breadboard prototype of a video encoder/decoder has been designed, constructed, and tested. The breadboard prototype will encode, transmit, and reconstruct real-time television pictures. Differential pulse-code modulation is used to reduce the digital data rate transmitted. The unit is self-contained and portable. Inputs and outputs, control switches, and light emitting diode displays are provided on the breadboard front panel. The internal construction of the breadboard is designed to provide simple access to all circuitry, and signals at every component can be easily monitored to facilitate system checkout and evaluation.

APPENDIX A

IMAGE CODING FOR A TIME MULTIPLEX COMMUNICATION LINK

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IMAGE CODING FOR A TIME MULTIPLEX COMMUNICATION LINK

1. INTRODUCTION

In digital data transmission systems, time multiplexing of digital data sources is often utilized to replace several parallel communication channels with a single communication link that is time-shared between the data sources. Application of time multiplexing to high bandwidth data sources, such as real-time television, is often limited by the extremely fast switching speeds of the multiplex and communication channel equipment. A solution to this problem is to perform image coding on the television signals prior to multiplexing in order to reduce the bit rate requirement of the communication system.

A block diagram of a time multiplex image coding system for three television sources is shown in Figure A-1. In operation, the analog signal of each camera is time sampled and digitally coded. The resultant code bits for each source are then grouped together and fed to a data multiplexer that forms a time sequence of data bits for the channel. At the receiver, the demultiplexer and decoders reconstruct the real-time television signals. The dotted lines between the coder blocks and decoder blocks indicate timing and control signals that provide time synchronization between the time samples of the three television sources. Also, additional cross-control may be used to provide more efficient coding. For example, code bits could be assigned between the three sources in proportion to the instantaneous information rate of each source.

Potential image coding techniques for a time multiplex communication link are reviewed in para 2. In subsequent paragraphs, the operation and performance of several linear predictive image coding systems that appear to be best suited for this application are described.

2. REVIEW OF POTENTIAL IMAGE CODING METHODS

Much literature on the subject of image coding exists (Reference A-1). Surveys of some of the most promising techniques are found in References A-2 through A-5. Image coding methods reviewed below are those techniques applicable to the coding of real-time, high-resolution, monochrome television for transmission over a time multiplex communication link. The design goal is at least a 4:1 bit rate reduction as compared to standard pulse-code modulation (PCM) coding at 8 bits per picture element (pixel). The fidelity criterion is subjective acceptability. It is assumed that the input to the coder is a standard analog television camera signal in NTSC format, including horizontal and vertical sync pulses, and that the decoder output must be a replica of the camera output video signal.

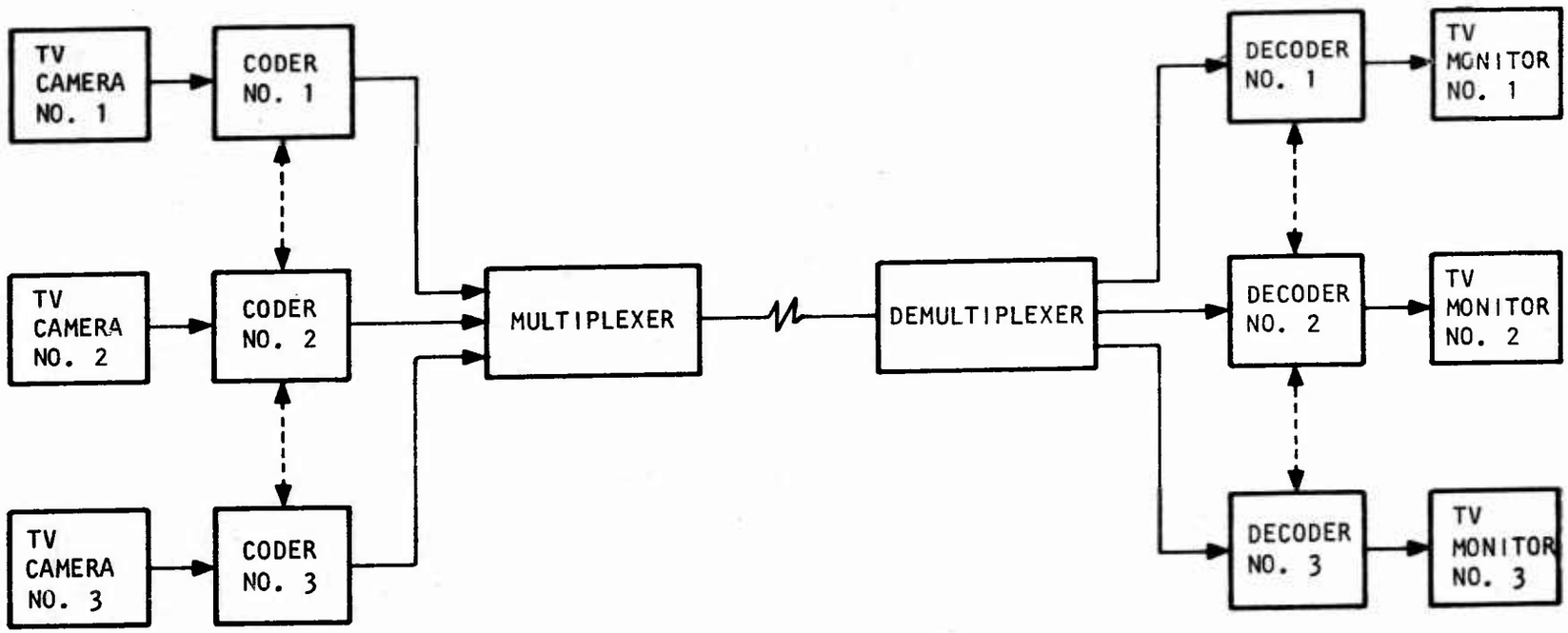


Figure A-1. Block Diagram of Time Multiplex Image Coding System

Many image coding methods are not considered because they are incompatible with the system requirements stated above. Systems that are potentially acceptable are listed below.

Picture interlace coding

Quantization reduction coding

Statistical coding

Predictive coding

Interpolative coding

Transform coding

Frame replenishment coding

These coding systems are analyzed and compared in the following paragraphs. A conventional PCM coding also is reviewed.

2.1 PULSE-CODE MODULATION CODING

In the basic PCM coding process, a video signal is time-sampled; each sample is quantized in amplitude, usually over a linear scale, and assigned a binary code word for transmission. Normally, uniform length codes are used for each brightness level; therefore, the number of brightness levels L is chosen to satisfy the relation

$$L = 2^b \qquad \text{(A-1)}$$

where b represents the number of bits allowed per image sample.

To achieve best results in digital television transmission, the video signal should be band-limited to some maximum cutoff frequency f_C and then time-sampled at a rate of at least twice the cutoff ($f_S = 2f_C$). If this procedure is followed, it is theoretically possible to reproduce an exact replica of the video signal from its time samples. Undersampling leads to two types of errors in reconstruction: (1) failure to accurately follow fast brightness changes and (2) the reconstruction of false, low-frequency signal components (aliasing error). The subjective effect of undersampling is dependent not only upon the sampling rate-to-cutoff frequency ratio (f_S/f_C), but also upon the shape of the video spectrum. If the video spectral energy drops off gradually, as is the case for most television cameras, the aliasing error effect will usually be negligible because the low-frequency picture artifacts will be of relatively low contrast. The quantization, coding, and reconstruction processes are illustrated in Figure A-2. In the PCM coder, comparator circuits determine the quantization band in which the video amplitude sample lies and cause the appropriate code word to be generated for transmission. At the PCM decoder, the amplitude of a reconstructed video pulse is set according to the received code word. Usually,

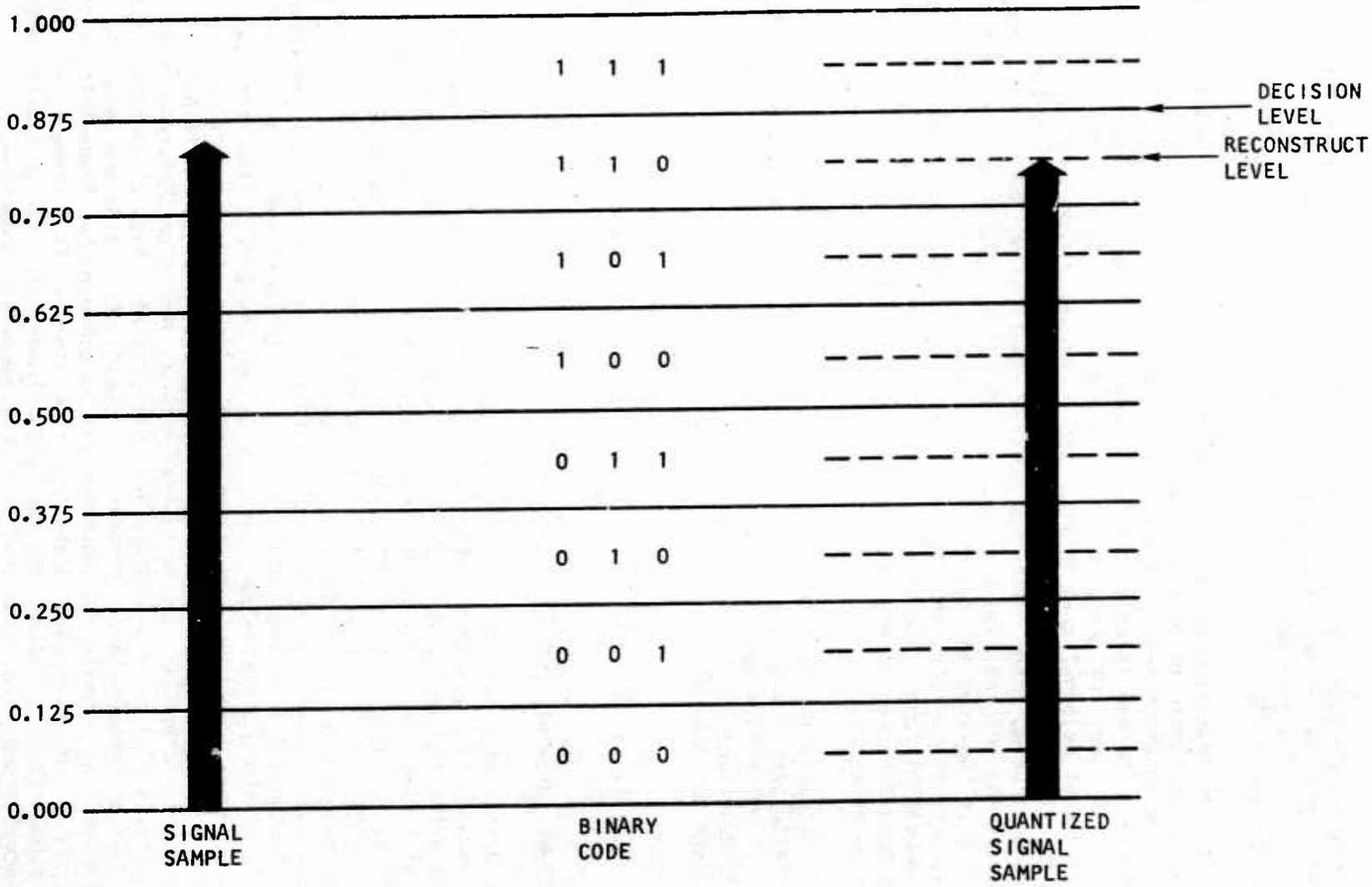


Figure A-2. Example of PCM Coding for 8 Level Code

the reconstruction level is set at the midpoint of the quantization band. If the video signal amplitude ranges from 0 to 1 units, the peak quantization error is $\pm 1/2L$. The root mean square quantization error for a uniform brightness distribution is $1/2\sqrt{3}L$.

A bit rate reduction can be achieved for PCM by the simple expedient of restricting the number of bits assigned to each sample. For subjective assessment, b (from Equation A-1) is lowered until the quantization effect becomes unacceptable. The eye is only capable of judging the absolute brightness of about 10 to 15 shades of gray, but it is much more sensitive to the difference in brightness of adjacent gray shades. For a reduced number of quantization levels, the first noticeable effect is a gray scale contouring caused by a jump in the reconstructed image brightness between quantization levels in an image region where the original image is slowly changing in brightness. The minimal number of bits required to prevent noticeable gray scale contouring depends upon a variety of factors, including the linearity of the camera and displays and the amount of camera and display noise. For low-quality cameras and displays, 5 to 6 bits may be adequate, while for high-quality instruments 7 to 8 bits may be necessary.

As a baseline for further discussion, a typical high-resolution, high-quality television system is considered. The cutoff frequency is assumed to be $f = 7.5$ MHz with a sampling rate of $f = 1.5 \times 10$ samples/sec. Each sample is quantized to 256 gray levels with an 8-bit code. The resultant channel rate for transmission is then

$$R = 1.5 \times 10^7 \frac{\text{samples}}{\text{sec}} \times 8 \frac{\text{bits}}{\text{sample}} = 1.2 \times 10^8 \frac{\text{bits}}{\text{sec}}$$

2.2 PICTURE INTERFACE CODING

The 2-to-1 line interlacing ratio used in conventional television was adopted because it provided a simple means of obtaining a 2-to-1 bandwidth reduction without objectionable flicker or image breakup. For television systems utilizing frame storage at the receiver, flicker is not a consideration. Thus, the only possible attribute of interlacing is its ability to provide a mechanism of bandwidth reduction without appreciable image breakup. The technique generally used for reducing bandwidth by 2-to-1 line interlacing is to scan every other line of a picture during one field, and scan the remaining lines in the next field. The field rate of the interlaced system is set at the frame rate of the noninterlaced system. To extend the 2-to-1 line interlace technique, for example, every fourth or eighth line would be scanned during a single field. The line interlace technique can be extended in the horizontal direction of a picture as well as in the vertical direction (Reference A-6). Conceptually, a picture frame is divided into several fields of picture elements or dots that are sequentially transmitted. Usually the fields are chosen to be nonoverlapping. A bandwidth reduction can be achieved by transmitting each field at the normal television frame rate. For example, if a frame is divided into 16 nonoverlapping fields, the equivalent frame rate will be one-sixteenth of the normal frame rate, resulting in a 16:1 bandwidth reduction.

The line and dot interlace systems of bandwidth reduction are subject to two types of optical disturbances in a displayed picture: (1) patterning and (2) dot crawl. Patterning is the optical illusion of a false texture in a picture due to the arrangement of dots within a frame. It is present when not all of the dots are displayed in a field period. The crawling effect is an optical illusion in which lines or dots of a picture appear to crawl across the display because of stroboscopic effects in the presentation of successive fields. It is possible to minimize these disturbing effects by properly ordering the successive presentations of picture fields with the content of each field judiciously arranged. From the standpoint of implementation, it is desirable to force a repetitive structure on the dot patterns and field presentation sequences. However, such structure must not be allowed to create patterning and dot crawl effects.

With a dot interlace system, the resolution of still scenes will be reduced by the interlace ratio unless the eye, display tube persistence, or an external memory provide some degree of field storage. For moderately low-frame-rate television systems, the eye and display tube persistence are inadequate storage mechanisms, and an external memory must be relied upon for field storage. With a memory used in the receiver system, each field that is not being replaced by "fresh" data may be taken from the memory and displayed on the monitor every display frame. Thus, full resolution for still scenes will be possible for complete storage of fields. However, this storage has a detrimental effect on the reproduction of moving objects in a scene because the field storage will cause smearing of an image of a moving object. The degree of smearing is directly proportional to the number of fields stored in the memory, but the number of stored fields also determines the resolution for still scenes. Thus, there is a compromise between the number of stored fields and the system resolution.

In summary, the dot interlace technique provides an effective means of bandwidth reduction for applications in which image motion is not great and some amount of artificial smearing of moving objects can be tolerated. The coder implementation is relatively simple, but a complete frame storage unit is required at the receiver.

2.3 QUANTIZATION REDUCTION CODING

Several methods have been proposed for the reduction of gray scale contouring when the number of quantization levels is limited. These methods are described below.

2.3.1 Pseudonoise Quantization

The visual effect of gray scale contouring can be minimized considerably by adding low-amplitude, pseudo-random noise to the video signal amplitude before quantization and synchronously subtracting the noise from the quantized video after the quantizer. This process, called Roberts' modulation (Reference A-7) after its developer, permits quantization with as few as 3 bits per sample without particularly noticeable gray scale contouring. However, there is an increase in the mean square error in the quantization process and an introduction of a snow-like visual degradation to the image.

2.3.2 Improved Gray Scale Quantization

In 1966, Bisignani, Richards, and Whelan (Reference A-8) introduced a quantization technique called the improved gray scale (IGS). In the IGS system, low-level brightness errors are introduced in certain elements to diminish the effect of gray scale contouring. These brightness errors are generated in a deterministic manner from the previous pixel (picture element) along the line. One version of the system operates as follows. Each pixel is uniformly quantized and assigned a 6-bit binary code. A construction code word is formed as the modulo 8 sum of the pixel code word and the three least significant bits of the previous construction code word. The addition is inhibited if the three most significant pixel bits are all ones. The three most significant bits of the construction code word are then transmitted, resulting in a 2:1 bit rate reduction.

The IGS code provides a display with only three bits, but the displayed value fluctuates more rapidly, and therefore tends to spread out the gray scale contours by spatial averaging within the eye. The mean square error of the reconstruction is increased somewhat compared to straight PCM coding. Pictures processed by the IGS system have diminished contouring, but exhibit a small scale graininess.

2.3.3 Coarse-Fine Quantization System

In the coarse-fine quantization system (Reference A-7), regions of the image that are not rapidly changing in brightness are represented with 6-bit accuracy. Brightness changes of less than one-eighth of full scale also receive a 6-bit representation, and large-amplitude, high-frequency brightness variations are coded with 3-bit accuracy. All displayed pixels are quantized to the full 64 levels.

In operation, the original image is linearly quantized with 64 levels and binary-coded with 6 bits per pixel. The three most significant bits form the coarse information, and the three least significant bits are the fine information. The basic coding concept is as follows. If the image is changing in brightness such that there is a change in the coarse bits, they are transmitted directly as absolute levels. However, if the coarse bits are not changing, the fine bits are transmitted as relative levels to be combined with the previous coarse bits to reconstruct a 6-bit pixel for display. Only three bits are transmitted for each pixel. The actual decision as to whether a pixel should be coarsely or finely represented is somewhat more complicated than described above. The decision is based upon a set of ad hoc rules utilizing the states of the past three pixels. Subjective testing has shown that the quantized images are equivalent in quality to 6-bit PCM images, except at edge regions where some gray scale contouring is noticeable.

In summary, the three quantization coding systems--pseudonoise quantization, improved gray scale quantization, and coarse-fine quantization--are simple, easily implemented techniques for reducing gray scale contouring while providing a 2:1 compression.

2.4 STATISTICAL CODING

Statistical measurements of the brightness distribution of digital images and subsequent entropy calculations indicate that the most natural images contain a large amount of redundancy. In this context redundancy can be defined as the total number of bits that are required for straight PCM coding minus the entropy of the entire image. The methods for designing codes to fully utilize this redundancy and to code an image with the same number of bits as its entropy are known in principle, but are generally not feasible to implement. It is possible, however, to eliminate some of the redundancy by simple coding techniques and achieve a worthwhile reduction in image transmission channel capacity requirements.

2.4.1 Single Pixel Coding

The simplest type of statistical image coder is one in which each pixel, in effect, is individually assigned a code group from a code book based upon its quantized amplitude. For efficient coding, the code assignment should be such that pixel values with a high likelihood of occurrence should receive code groups with a few number of bits, and conversely, rare pixel values should be assigned the longer code groups. If this process is performed efficiently, the average length of a code group will be equal to the single pixel entropy of the image. For typical natural monochrome images quantized to 64 levels, the single pixel entropy ranges from about 4 to 6 bits per pixel. This relatively small amount of redundancy as compared to 6-bit-per-pixel constant word length PCM coding (providing at most a 1.5:1 compression) is seldom worth the penalty of increased implementation requirements and the general difficulties associated with variable length codes.

2.4.2 Pixel Difference Coding

Since adjacent pixels along an image line are highly correlated in natural images, a high degree of redundancy exists between pixel pairs along a line. This redundancy can be utilized by coding the running differences between pixels along a line. If each pixel has L quantization levels, then the pixel difference may assume any one of 2L-1 values. Since the probability of occurrence of large differences is relatively small, it is possible to simplify the coder considerably without a great loss in performance. The coding strategy is as follows. Small differences receive individual code words. If the differences exceed some specified level, the actual pixel value is coded and appended to a prefix code that distinguishes the total code words from the coded differences. A code of this nature can provide a 2:1 bandwidth compression with no coding error (Reference A-9).

2.4.3 Run Coding

In an intraframe run coding system, the amplitudes of adjacent pixels along a line are compared. If a significant change in detail (for simplicity, called an edge) occurs, a run is said to exist. Either a function of the amplitude of the brightness of the pixel at the end of the run or a function of the amplitude of the difference signal is transmitted along with an indication of the location of the run end. If the location of the end of the run is

determined by counting the number of elements from the beginning of the line to the occurrence of the end of the run, the system is called run-end coding. The location of the end of a run also can be specified in terms of the relative distance from the previous run end. This system is denoted as run-length coding.

For a digital transmission system, the amplitude and position of a run are transmitted as a group of code bits. If the amplitude and position of the runs are to be transmitted as they occur in a continuously scanned image, a reduction of the transmission signal power density will be possible, but the bandwidth will be unchanged. To achieve a bandwidth reduction it is necessary to gather the runs of a picture and redistribute them in a transmission time sequence at a rate that is equal to the average rate of their occurrence. This can be accomplished with a memory at the camera which stores the amplitude and position of runs, or by using a stop-scan system which generates runs at a fixed rate (Reference A-10). The run-length coding system has been found to be practical only for black or white facsimile signals. If the image contains many gray scales or if the image sensor is noisy, the compression ratio achievable is seldom greater than 2:1, and there is a noticeable loss in high-frequency detail.

2.4.4 Bit Plane Coding

In constant word length PCM coding of an image, the code words may be conceptually organized into planes corresponding to their pixel position, with the most significant bits occupying the lower plane. In most natural images, the lower plane bits seldom change, while the upper plane bits fluctuate almost randomly. In principle, a bandwidth reduction is possible by run-length coding the bit state transitions in each bit plane. However, simulation tests indicated that the bandwith reduction obtainable is usually much less than 2:1.

2.5 PREDICTIVE CODING TECHNIQUES

In basic predictive coding systems such as that shown in Figure A-3, a predictor weights pixels along a line (or prior lines that have been previously coded) and generates an estimate of the present pixel. The difference between the estimate and present pixel value is quantized, coded, and transmitted over the channel. At the receiver, the quantized prediction error is used to reconstruct an estimate of the present pixel value for display. The advantages of predictive coding compared to straight PCM coding are (1) the differential signal is less correlated than the original pixel signal and can therefore be coded more efficiently; (2) the differential signal has a smaller variance than the direct pixel signal, and the quantization noise (which is proportional to the variance of the signal to be quantized) is smaller; and (3) the probability density function of the differential signal is less subject to variations in image content, and hence the quantizer can be designed more efficiently. Several image coding systems based upon the principle of predictive coding are described below.

2.5.1 Deltamodulation

The deltamodulation image coder is a special type of linear predictive coder in which the quantizer of Figure A-3 is restricted to two levels and the predictor is a one-pixel period time delay device (Reference A-11). In

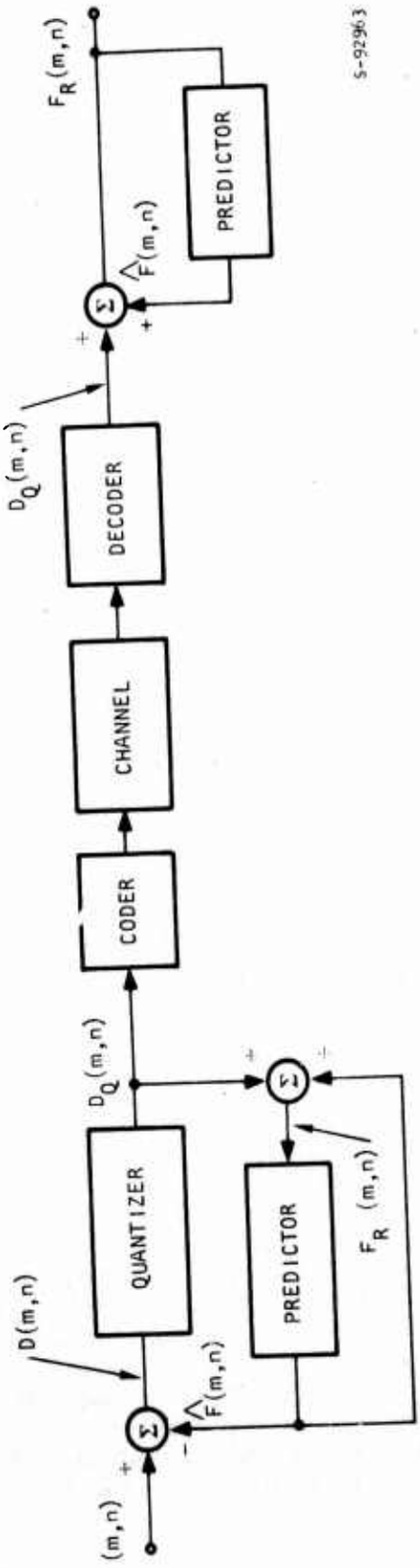


Figure A-3. General Predictive Image Coding System

operation, a pixel sample is fed to a summing unit that forms a difference signal proportional to the difference between the present pixel value and its estimate obtained from the predictor circuit. If the difference signal is positive, a positive pulse of a given step size is produced; otherwise, a negative pulse is produced. The positive and negative pulses are then represented as "one" and "zero" binary bits and transmitted. At the same time, the quantized difference pulses are fed back to the predictor, which forms the estimate for the next pixel to be scanned. In effect, the estimate is a stepwise representation of the input video signal delay by a pixel period. The deltamodulation receiving system sequentially receives the code bits and reconstructs the positive and negative difference pulses, which are summed with the receiver estimate of the pixel signal to produce a reconstructed image pixel value. A low-pass filter removes spurious high-frequency components of the reconstructed video signal.

Typical waveforms in a deltamodulation system are illustrated in Figure A-4. This figure also indicates a basic problem of the deltamodulation system. If the quantizer step size is kept small to minimize the quantization error, then video slopes with fast rise times cannot be accurately followed unless the sampling rate is very high. Thus, for a fixed sampling rate a tradeoff exists between quantization error and the slope overload effect. Results of a computer simulation of a deltamodulation coder are given in Figure A-5. The original image is PCM-coded at 8 bits/pixel and contains 256 by 256 pixels. In the example in which the quantization step is set at 5 percent of the full-scale video amplitude, the effect of slope overload is quite noticeable. On the other hand, for a step size of 20 percent, the effect of quantization granularity is pronounced. A best compromise based upon subjective evaluation is a step size of about 10 percent.

One means of reducing the slope overload without increasing the quantization error is to permit the deltamodulation system to assume more than two levels. Multilevel deltamodulators do indeed achieve better performance, but at the cost of additional complexity. A multilevel deltamodulator is really a special case of a differential PCM coder. Another method of reducing slope overload is to perform sampling at a higher rate. However, studies have shown that it is more effective to maintain sampling at the Nyquist rate and increase the number of quantization steps for the difference signal (Reference A-12).

2.5.2 Differential Pulse-Code Modulation

A differential pulse-code modulation (DPCM) coder operates in the same manner as a deltamodulation coder except that the difference signal is quantized to multiple levels (usually eight) rather than only two levels (Reference A-4). A tapered quantizer scale (as shown in Figure A-6) provides a smaller mean square reconstruction error than a linear scale. Also, subjective performance is improved because the eye is relatively insensitive to errors in large amplitude edges within a picture. Studies have shown that DPCM coding of individual pictures with an eight-level tapered quantizer and a 3-bit/pixel code provides good quality results (Reference A-12). However, for real-time television the residual slope overload errors from individual frames tend to interact somewhat and produce a degradation called edge busyness. This edge busyness appears as a sparkling in the vicinity of edges.

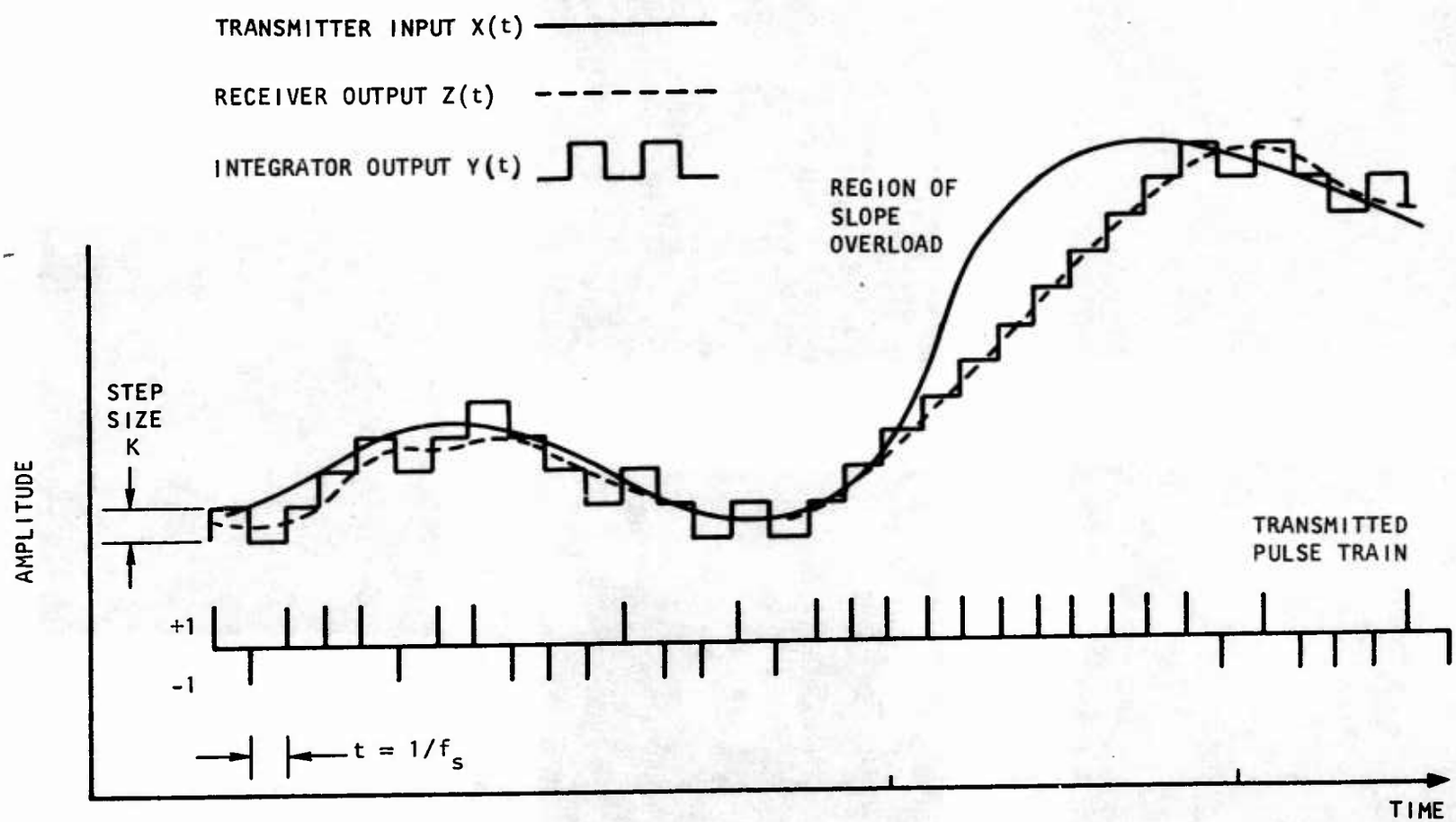


Figure A-4. Typical Signals in a Deltamodulation System

a. ORIGINAL PCM 256 x 256 PIXELS, 8.0 BITS/PIXEL

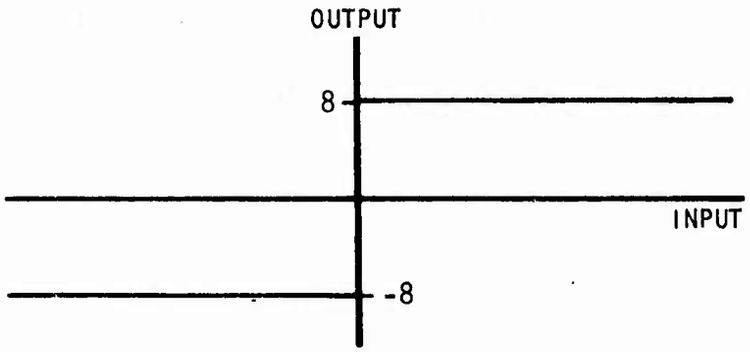
b. DELTAMODULATION q = 5 PERCENT, 1.0 BITS/PIXEL

c. DELTAMODULATION q = 10 PERCENT, 1.0 BITS/PIXEL

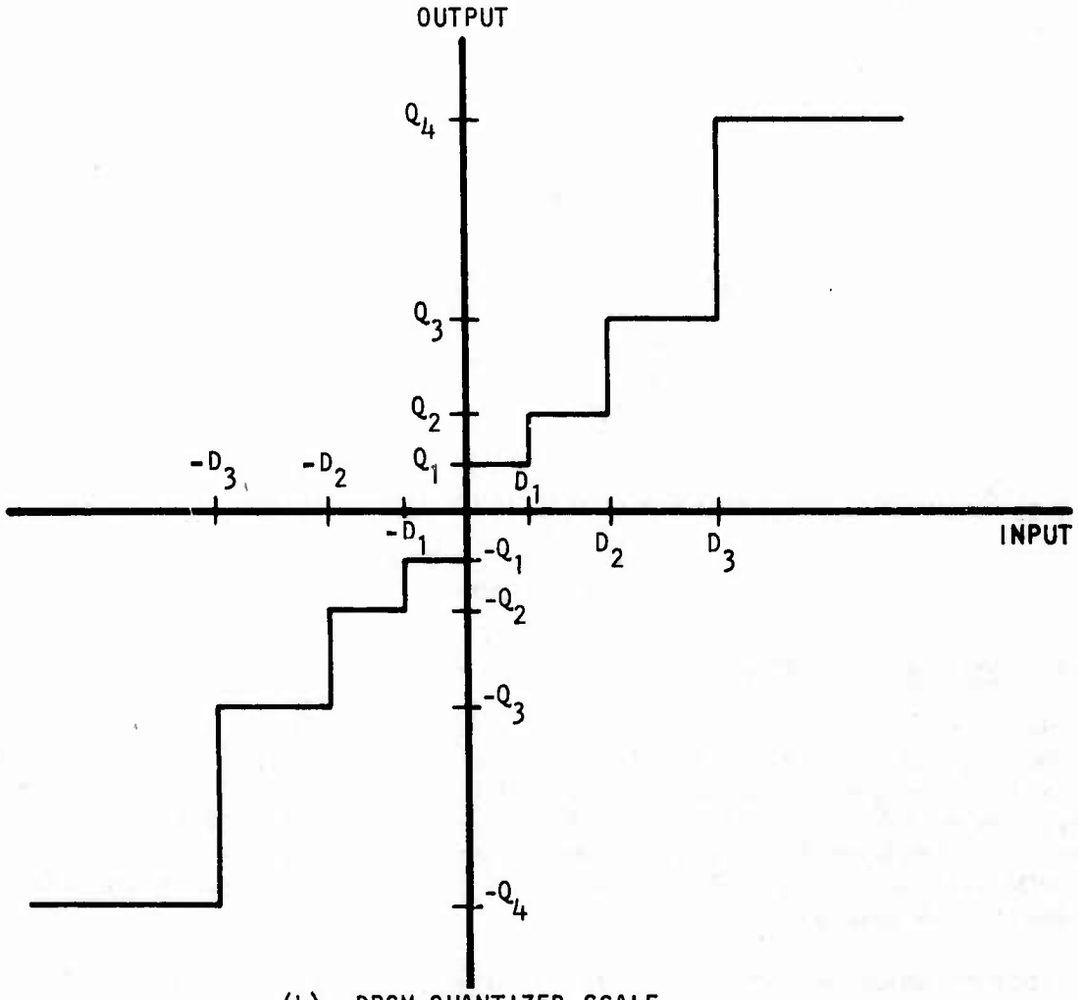
d. DELTAMODULATION q = 20 PERCENT, 1.0 BITS/PIXEL

e. DPCM Q_1 = 2.5 PERCENT, 3.0 BITS/PIXEL

Figure A-5. Computer Simulation of Deltamodulation and DPCM Image Coding Systems



(a) Deltamodulation Scale



(b) DPCM QUANTIZER SCALE

Figure A-6. Deltamodulation and DPCM Quantizer Scales

The results of a computer simulation of a DPCM coder is given in Figure A-5e. In this example, the eight-level quantization scale of Figure A-6 was employed with the lowest quantization step set at 2.5 percent full-scale.

2.5.3 Spatial Predictive Coding

In a basic DPCM image coder, the quantized difference signal between the actual pixel value scanned and the previously scanned pixel is used as the basis of the feedback prediction. This feedback prediction can be improved by using the quantized difference signals of several neighboring pixels as shown in Figure A-7. An improved feedback estimate reduces quantization error, which in turn leads to improved image quality (Reference A-13). The drawback of a spatial predictive coder is implementation complexity. Utilization of previous line data in the prediction requires a one line storage unit. Also, the structure of the predictor is more complex than a DPCM predictor.

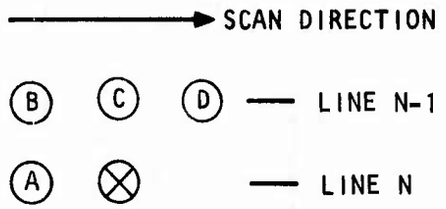


Figure A-7. Relationship of Pixels in a Spatial Predictive Coder

2.5.4 Adaptive Predictive Coders

Reconstruction errors in a predictive image coding system can be reduced by adapting the quantizer scale to the dynamic image activity. For example, if the image brightness along a line is changing rapidly, the quantization levels can be decreased to reduce granularity error. This technique has been effectively used for several adaptive deltamodulation systems (Reference A-14). For DPCM systems, the amount of improvement has not proven worth the additional implementation complexity.

Another adaptive technique that has been proposed is the dual-mode DPCM deltamodulation coder in which the coder operates in either a DPCM or deltamodulation mode (Reference A-15). If the image brightness is relatively smooth over several samples, the image is coded by deltamodulation at 1 bit/pixel, and if the brightness changes abruptly, the coder switches to 3-bit/pixel DPCM until the image activity once again reduces to a smooth level. With such a system, good quality results can be obtained at about 2 bits/pixel.

2.6 INTERPOLATIVE CODING

Interpolative coding systems are based upon numerical representation or approximation techniques whereby a sequence or plane of pixel values is fit by continuous functions. There are two basic interpolation processes that can be applied to image coding: receiver interpolation and transmitter interpolation. These are described below.

2.6.1 Receiver Interpolation

A 2:1 bandwidth reduction can be obtained simply by transmitting only odd-numbered lines of an image frame and then artificially generating the even lines by interpolation functions at the receiver. Alternatively, the original image could be sampled in a checkerboard pattern, and the missing pixels could be interpolated at the receiver by a two-dimensional interpolation function. A television processing system utilizing receiver interpolation to provide bandwidth reduction has been developed by Gabor and Hill (Reference A-16). In this system, fields are transmitted at low rates, and at the receiver, interleaving fields and frames that are based upon the transmitted field are artificially synthesized and displayed. The method of generating the interleaved fields and frames is called contour interpolation. The process only provides an approximation of an image, and may result in large reconstruction errors.

2.6.2 Transmitter Interpolation

The transmitter interpolation system is based upon the approximation of a scan line of image data by line segments. An example of interpolation using straight line segments is given in Figure A-8 (from Reference A-17). In the most general form, the segments can be of any shape and lie anywhere within some error bounds about the image data. Simplifications are usually made by (1) restricting the line segments to straight lines, (2) requiring the line segments to be connected, and (3) anchoring the line segments to image samples. Even with all of these simplifications, the coding operation is rather complex. Interpolative coders have been simulated on a computer and shown to provide excellent quality images at compression ratios of up to 6:1, but it does not appear feasible to implement such a system for real time television.

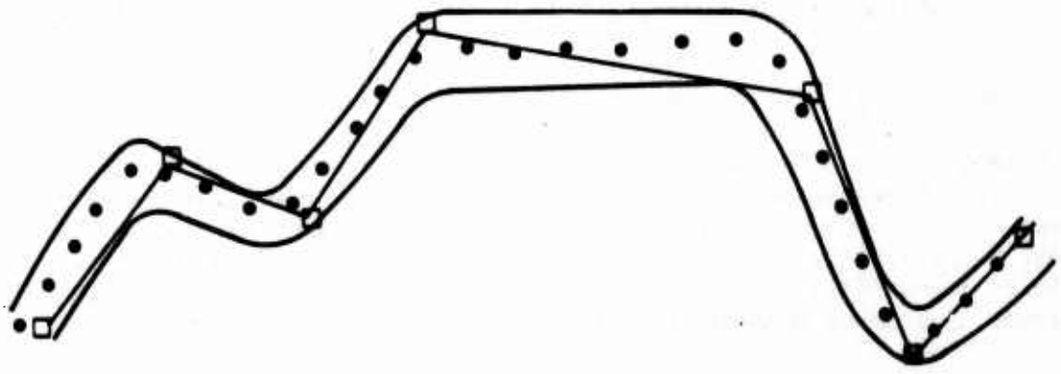


Figure A-8. Example of First-Order Interpolator

2.7 TRANSFORM CODING

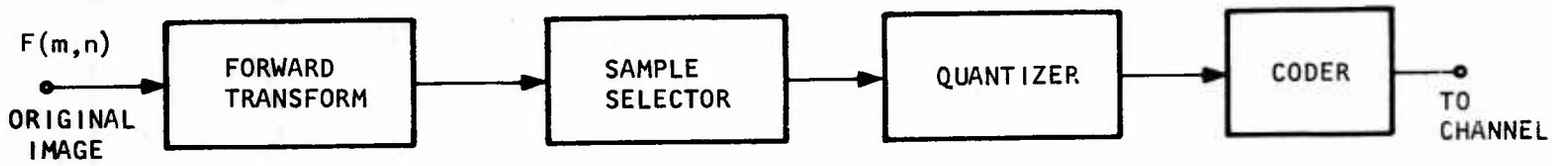
A block diagram of a transform coding system for monochrome images is shown in Figure A-9. In operation, a two-dimensional mathematical transform is taken of the image pixels over the entire image or repeatedly over some subsection of the image (called a block). The transform domain samples are then quantized, coded, and transmitted over the channel. At the receiver, the data are decoded to reconstruct the transform domain and an inverse transformation is performed to reconstruct the original image.

The mathematical transforms that have been utilized for transform image coding include Fourier, Hadamard, Karhunen-Loeve, Haar, and Slant. (References A-18 through A-21). Each of these transforms has the property of compacting the energy in the image domain to a relatively few number of transform domain coefficients. A bandwidth reduction compared to straight PCM may be achieved by efficient quantization and coding of the transform samples while maintaining the mean square reconstruction error below some acceptable limit. There are two basic methods of transform coding: (1) zonal coding and (2) threshold coding. Zonal coding entails the establishment of zones in the transform domain. In each zone every transform coefficient is quantized according to some scale, which is usually nonlinear, and then assigned a code group. A more efficient variant of zonal coding is to assign an average code length to each zone and use variable-length Huffman coding of the quantized samples. In either case the bit assignment is based upon the assumed variance of the transform domain samples. An example of the comparative performance of the various image transforms as a function of the image block size is given in Figure A-10 for a simple coding algorithm that gives a 4:1 compression. As shown, less than 1 percent mean square error can be achieved with the transforms for image blocks of about 16 by 16 pixels. The second type of transform domain coding -- threshold coding -- is based upon the establishment of a magnitude threshold. If the transform coefficient magnitude is greater than the threshold, it is quantized and coded; otherwise, it is discarded. It is necessary to code the location of the significant coefficients as well as their amplitude. With either zonal or threshold coding, it is possible to achieve bandwidth compressions of from 4:1 to 6:1 with good quality reconstructions. Even with compressions of on the order of 25:1, the reconstructed image is still recognizable.

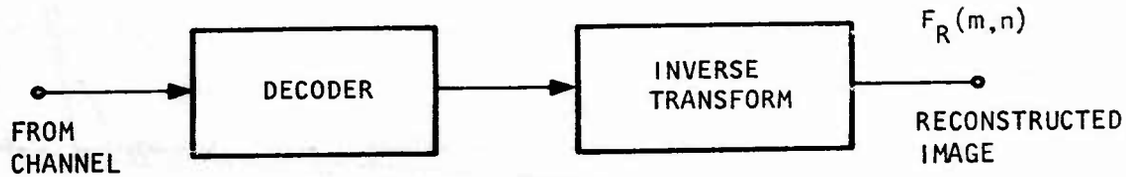
One of the major drawbacks of transform image coders in the past has been their implementation complexity. However, new technologies have emerged, and for future applications, it appears possible to implement a transform coder for real-time television signals by the use of charge-coupled devices. (Reference A-22).

2.8 FRAME REPLENISHMENT CODING

A large television bandwidth reduction could be realized if spatial redundancy between adjacent frames of television pictures could be removed. In most scenes there is relatively little change in detail between adjacent frames; thus, by only transmitting the change in detail referenced to an initially transmitted frame, a significant bandwidth compression may be realized. The basic problem with this concept is the development of a



(a) TRANSMITTER UNIT



(b) RECEIVER UNIT

Figure A-9. General Transform Image Coding System

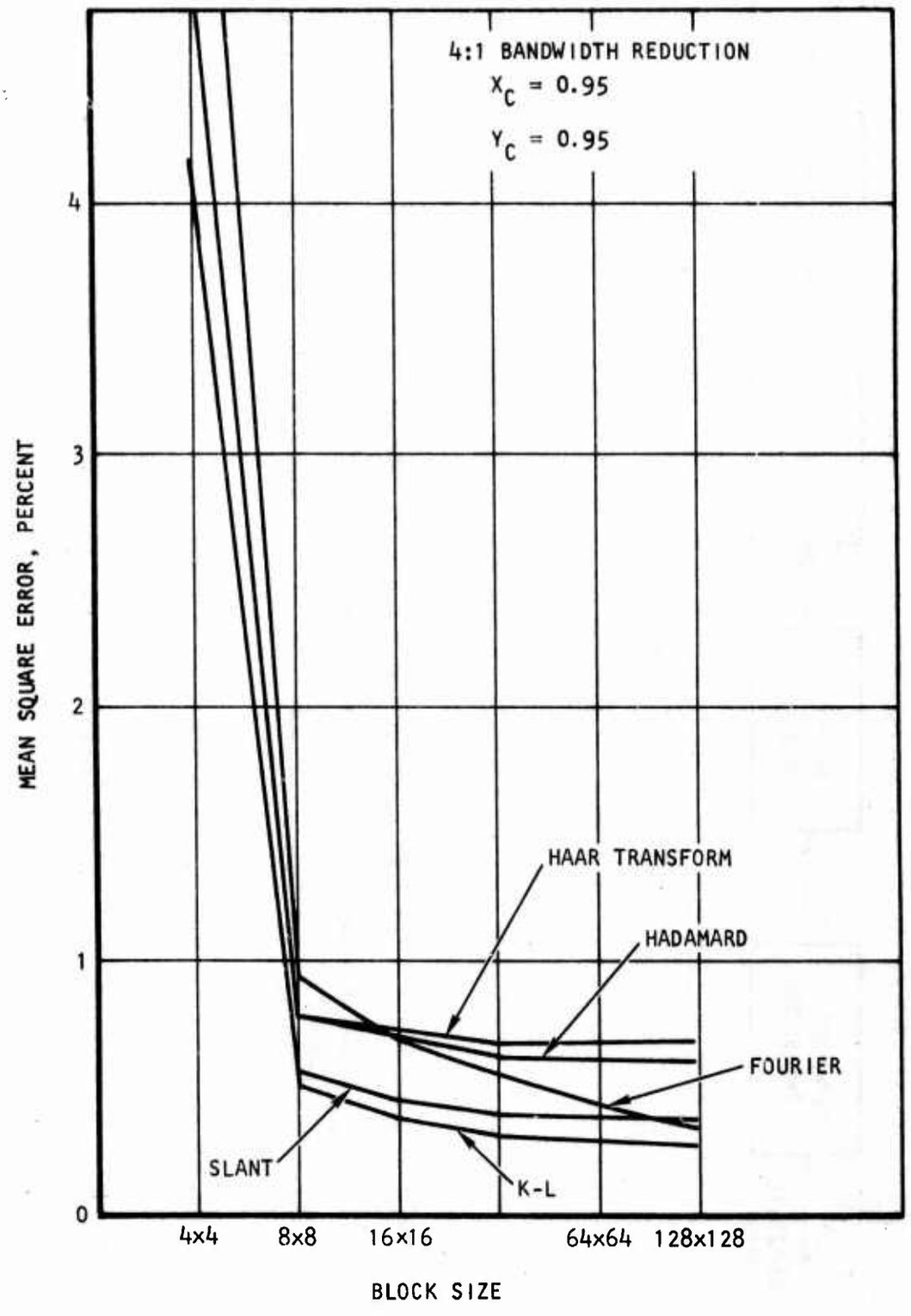


Figure A-10. Mean Square Error Performance of Transform Image Coders

method of making the frame detail difference signal consistent with the picture scanning and transmitting processes, using a modest amount of signal storage and processing equipment. If the pixel differences are formed between adjacent frames, a majority of the elements are virtually unchanged. This observation led to development of a frame-to-frame coding technique by Mounts (Reference A-23) -- replenishment coding. This system can be considered as a form of run coding applied between frames rather than along lines.

A block diagram of the frame replenishment coding system is given in Figure A-11. In operation, each camera frame is digitized with 8 bits and the first frame of the sequence is digitally stored in a reference frame memory. In subsequent frames, each digitized pixel is compared to its counterpart in the frame memory. If a significant difference exists, the new pixel value replaces the stored value in the frame memory, and is also placed in a buffer memory for transmission. It is also necessary to identify the position of the significant change along the line by its horizontal code coordinate. The first pixel along each line is so coded to provide a line count. To prevent overflow of the transmitter buffer, the allowable difference signal that causes a new pixel to be coded is varied as a function of remaining buffer capacity. If the buffer is nearly empty, the replenishment sensitivity is set low; conversely, if the buffer is close to capacity, the replenishment sensitivity is increased. Simulations of this system have been made by production of a movie. Coding of about 1.0 bit/pixel can be achieved at the expense of some edge rendition degradation. Also, if the subject moves quite rapidly within the scene, buffer overflow will occur, with a resultant smearing of the reconstructed image.

2.9 COMPARISON OF POTENTIAL IMAGE CODING METHODS

A performance summary of the image coding methods described above is given in Table A-1. The source rate is stated in terms of the average number of code bits per pixel. As a reference, conventional PCM requires from 6 to 8 bits per pixel. The design requirement for the image coding system of the time multiplex communication link is a 4:1 bit rate compression, or equivalently, a source rate of 2.0 bits/pixel. Consequently, the quantization reduction coding and statistical coding methods listed in Table A-1 are dropped from further consideration because their source rates are too high. The dot interlace and frame replenishment methods have been eliminated because of their frame storage requirements. The transmitter interpolation coding method and the transform coding methods are quite complex to implement with conventional circuitry. Real-time operation of an interpolative coder is not possible; real-time operation of a transform coder has been demonstrated only for relatively small image blocks for which the coding error is large. Thus, these methods also have been dropped from further consideration. There has been considerable progress toward the development of transform coders using charge-coupled devices. When this technology is fully developed, the cost, weight, and volume of a transform coder should be no greater than that of a linear predictive coder.

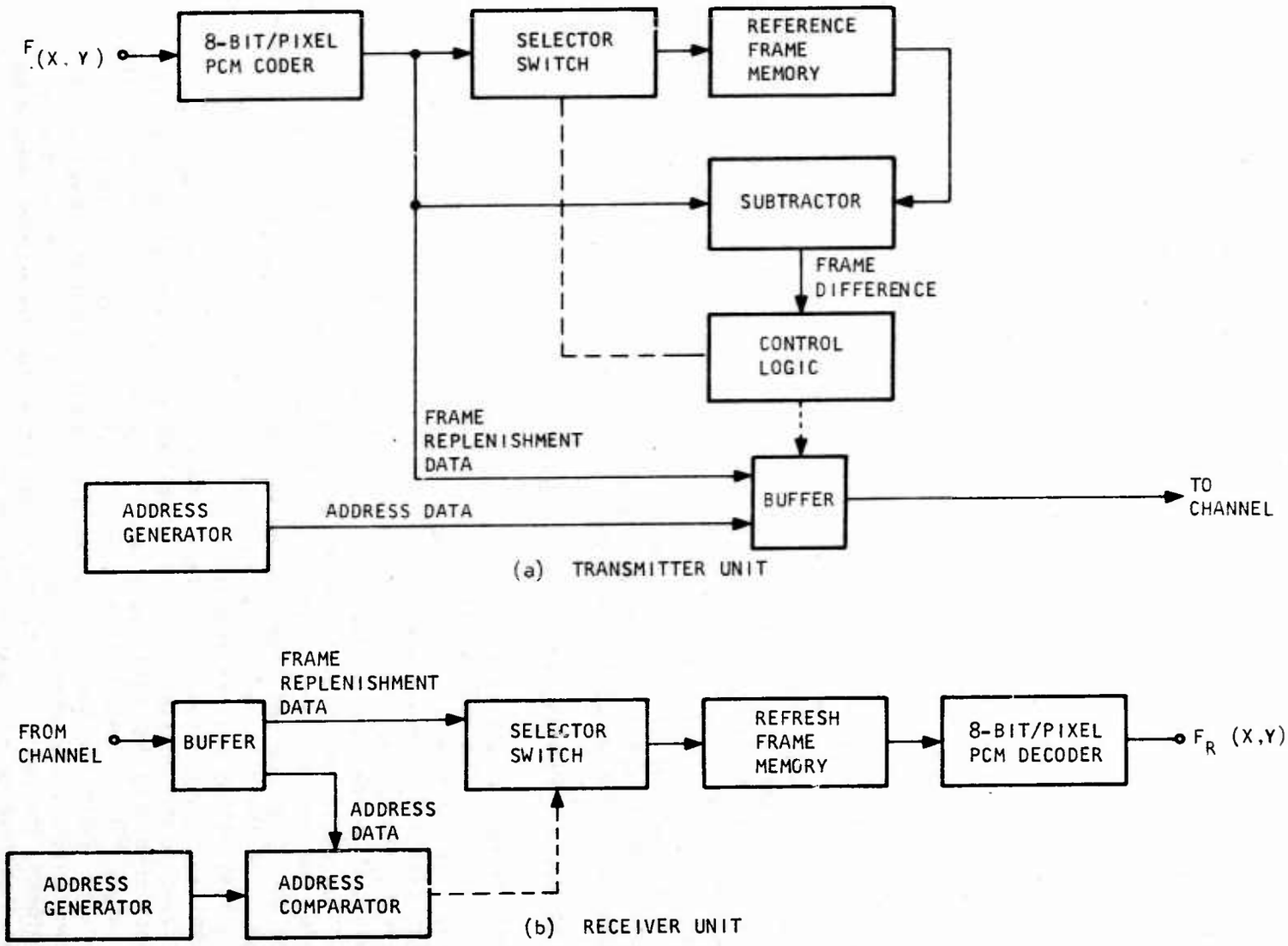


Figure A-11. Frame Replenishment Image Coding System

TABLE A-I. IMAGE CODING METHODS

System	Source rate, bits/pixel	Comments
16:1 dot interlace	0.5	Spatial smearing at high compression factors; receiver frame storage requirement.
Pseudonoise quantization	3.0	Snow-like interference; simple implementation.
Improved gray scale quantization	3.0	Residual gray scale contouring; simple implementation.
Coarse-fine quantization	3.0	Gray scale errors in vicinity of edges; simple implementation.
Previous pixel coding	3.0 to 4.0	Information preserving; moderate implementation; line buffer required.
Run coding	1.5 to 3.5	Edge degradation and gray scale contouring; moderate implementation; line buffer required.
Deltamodulation (ΔM)	1.0	Slope overload and granularity errors; simple implementation.
DPCM and spatial	2.0 to 3.0	Good quality but some edge busyness unless high-order prediction and adaptive quantization is used; moderate implementation complexity.
Dual-mode DPCM/ΔM	2.0	Same quality as DPCM; moderate to complex implementation; line buffer required.
Transmitter interpolation	2.0	Good to excellent quality; very complex implementation.
Zonal transform coding	1.5 to 2.0	Good to excellent quality; complex implementation.
Threshold transform coding	1.0 to 1.5	Good to excellent quality; very complex implementation.
Frame replenishment coding	1.0 to 1.5	Good quality; complex implementation; frame storage requirement

The remaining methods given in Table A-1 that are feasible for the time multiplex communication link application from the standpoint of source rate performance and simplicity of implementation are the linear predictive coding techniques. Deltamodulation provides the lowest source rate (1.0 bit/pixel), but its coding quality is relatively poor. Coding at 2.0 bits/pixel can be obtained with reasonable fidelity with special forms of DPCM, spatial predictive coding, or dual mode DPCM/deltamodulation coding. These systems are considered in greater detail in the following paragraphs.

3. DIFFERENTIAL PCM CODING TECHNIQUES

Conventional DPCM coding systems employ Nyquist rate sampling with each difference signal quantized to eight levels and coded with a constant length code of 3 bits. Thus, the source coding rate is 3.0 bits/pixel. Several approaches could be used to reduce this rate to the 2.0 bits/pixel required for the time multiplex communication link. These are:

(a) Reduce the number of quantization levels from 8 to 4

(b) Reduce the number of quantization levels from 8 to 6 and employ variable length coding

(c) Reduce the sample rate by a factor of two-thirds

(d) Time-multiplex quantizers between the three parallel channels

The first approach would lead to significantly greater slope overload error and granularity error because of the reduced number of quantization levels. With the second approach, the slope overload and granularity errors would be increased somewhat, and perhaps could be limited to tolerable levels. However, it would be necessary to provide line buffering at the coder and decoder because of the variable-length code. The concept of undersampling by the two-thirds factor is appealing from the standpoint of simplicity. Effects of undersampling are considered below. The fourth approach of a time-shared quantizer also is attractive because the implementation is quite simple. This system also is analyzed below.

In the undersampled DPCM system, the video signal is sampled at two-thirds its normal rate, and each DPCM difference sample is coded with a uniform-length 3-bit code. As a result, the average source rate referred to Nyquist samples of the video signal is 2.0 bits/pixel. The effect of undersampling will be to reduce horizontal resolution. Aliasing error can be eliminated, or at least reduced substantially, by proper prefiltering of the video signal before it enters the DPCM coder. To aid in assessing resolution loss, a block diagram of a system for pre-filtering and sampling a video signal is given in Figure A-12. In this system, a video signal $v(t)$ with an extended power spectrum $W(f)$ enters a pre-sampling filter with a sharp frequency cutoff at f_c. The function of the pre-sampling filter is

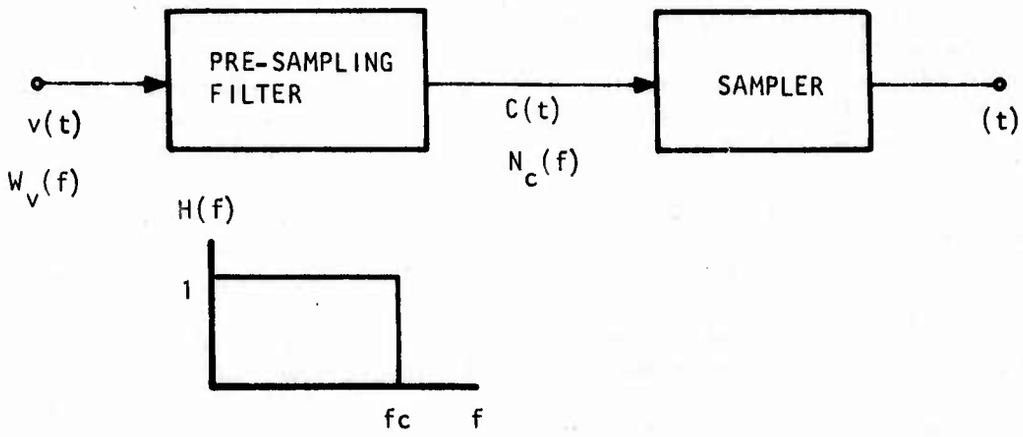


Figure A-12. Pre-Sampling Filtering of a Video Signal

to band-limit the input video signal and eliminate aliasing error in the following sampling process. For analytical simplicity, it will be assumed that the frequency cutoff of the pre-sampling filter is sufficiently sharp such that

$$W_c(f) = W_v(f) \qquad f \leq f_c \tag{A-2a}$$

$$W_c(f) = 0 \qquad f > f_c \tag{A-2b}$$

If sampling is to be performed at two-thirds the Nyquist rate, then the cutoff of the pre-sampling filter also must be reduced by two-thirds to prevent aliasing. There will be a resulting loss in horizontal resolution. One measure of this loss is to compute the relative energy difference between the spectra for the cutoff filter set at the Nyquist cutoff and attwo-thirds the Nyquist cutoff. The percentage resolution loss so defined is

$$R = \frac{\int_{2/3 f_c}^{f_c} W_v(f)\,df}{\int_0^{f_c} W_v(f)\,df} \tag{A-3}$$

It is necessary to measure and estimate (or model the power spectrum of typical television imagery. A common model is based upon the assumption that the correlation between points along an image line is exponentially related to their separation. The resulting power spectrum of the video signal then assumes the form

$$W_v(f) = \frac{A}{1 + \left(\frac{f}{f_o}\right)^{2m}} \tag{A-4}$$

where f_o is the half-power point frequency and m is an integer governing the rate of fall off of the frequency spectrum. A plot of resolution loss for this model when the cutoff filter is reduced to two-thirds its normal value is given in Figure A-13. A computer simulation has been performed to assess resolution loss. The results (shown in Figure A-14) show a perceptible loss of high-frequency detail, but all objects are clearly identifiable.

In the coding of real-time NTSC television signals, the horizontal and vertical sync pulses can be stripped from the composite video signal prior to coding and then reinserted at the receiver after decoding. Horizontal and vertical sync digital codes must be inserted in the bit stream of the television coders to provide proper timing for insertion of the sync pulses at the receiver. An alternate approach that reduces the implementation complexity of the coding system is to completely code the composite NTSC signal. An important consideration then is the effect of coding on the horizontal and vertical sync portions of the composite video signal. The results of a computer simulation of the coding of a horizontal sync pulse by the undersampled DPCM coder are shown in Figure A-15. The small amount of slope overload error of the DPCM coder does not appear to appreciably affect the rise and fall of the sync pulse. Also, the granularity error on the flat portions of the sync pulse is not severe. Subsequent smoothing by the video reconstruction filter will further reduce the granularity error. Thus, the computer simulation indicates that it is possible to code the composite video signal if desired. A disadvantage of this approach, however, is that in an NTSC composite video signal, the video voltage range is 1.0 v and the sync pulse excursion adds another 0.5 v to the range. Thus, if the composite video signal is to be coded, the total input signal range is 50 percent larger. This results in somewhat greater slope overload and granularity error in the video signal portion of the composite signal.

4. DUAL-MODE DPCM/DELTAMODULATION IMAGE CODING METHODS

In 1971, Frei, Vettiger, and Schindler (Reference A-15) published a paper describing a dual-mode DPCM/deltamodulation image coding system in which the coder operates in a deltamodulation mode in regions of relatively constant image brightness and switches to DPCM if the brightness changes at a high rate. With this coding system, good quality picturephone-type imagery was obtained at an average coding rate of 2.0 bits/pixel. The encouraging results obtained with the dual-mode coder for picturephone images by Frei, et al, prompted an investigation of its use for the transmission of high-resolution imagery over a time multiplex communication link. Several versions of the dual-mode coder are described below.

4.1 BASIC DUAL-MODE CODER

A block diagram of a basic dual-mode image coding system is shown in Figure A-16. In operation, an image sample is fed to a summing circuit that forms the difference between the pixel value and its estimate obtained from a feedback circuit. The difference signal enters a ten-level quantizer circuit that has the transfer function indicated in Figure A-17. If the coder

$$N_v(f) = \frac{A}{1 + (\frac{f}{f_o})^2}$$

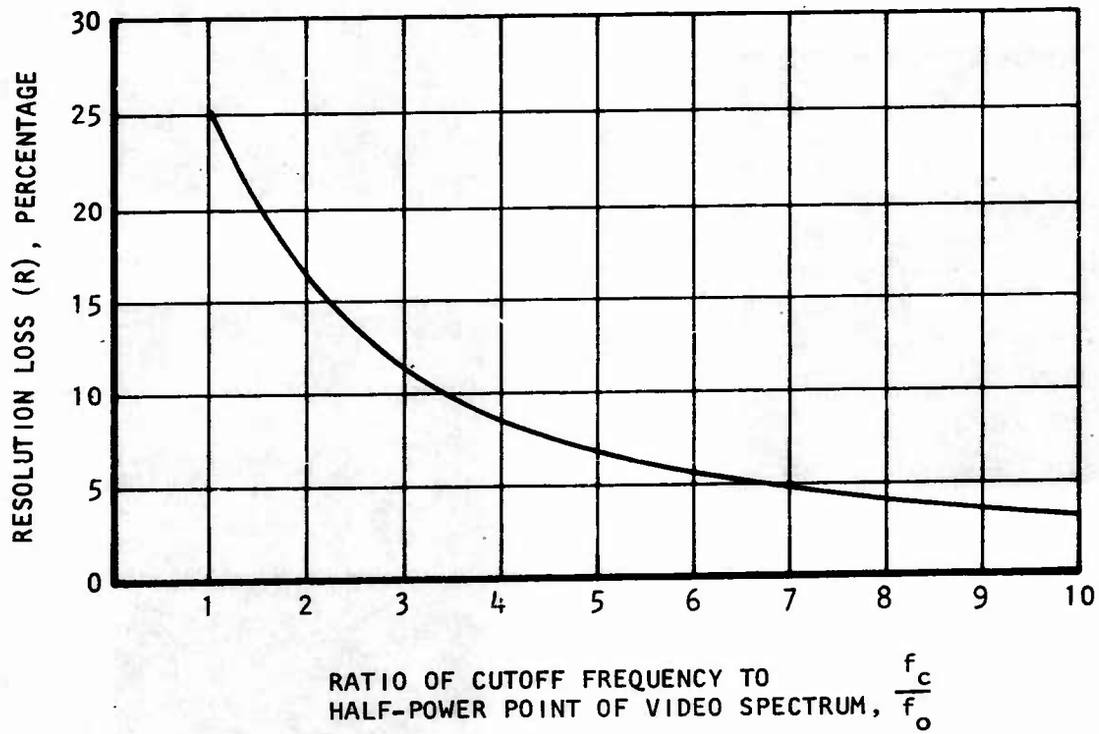


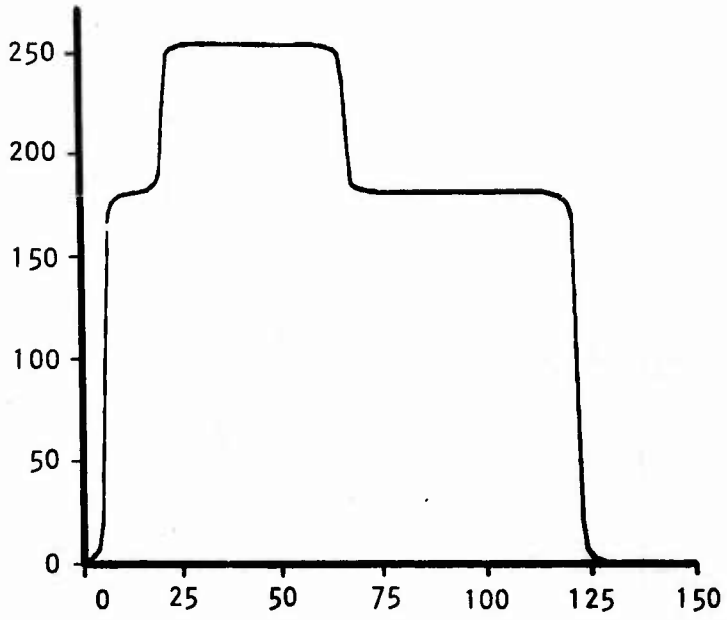
Figure A-13. Resolution Loss Resulting from Sampling at Two-Thirds Nyquist Rate

a. ORIGINAL PCM
512 x 512 PIXELS
8.0 BITS/PIXEL

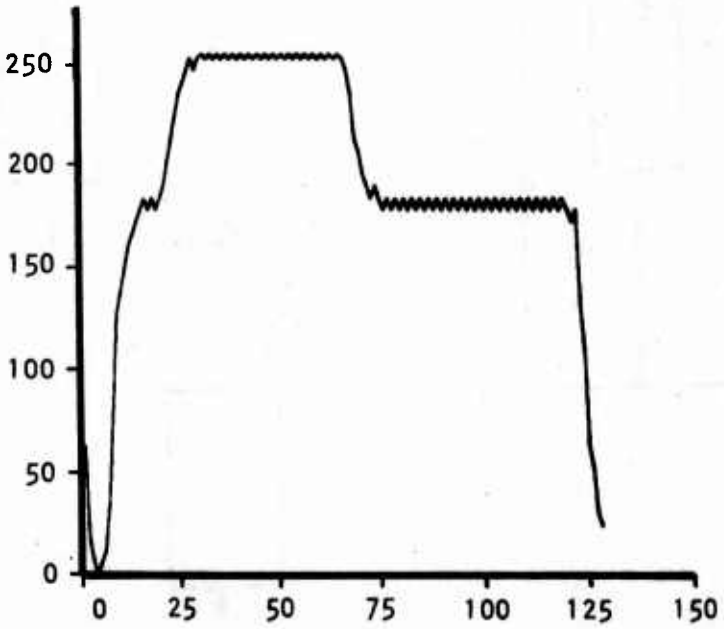
b. BANDLIMITED
PCM ORIGINAL
TWO-THIRDS NYQUIST
SAMPLING

c. DPCM CODING OF (b)
AVG. 2.0 BITS/PIXEL

Figure A-14. Computer Simulation of DPCM For Two-Thirds Nyquist Sampling Rate

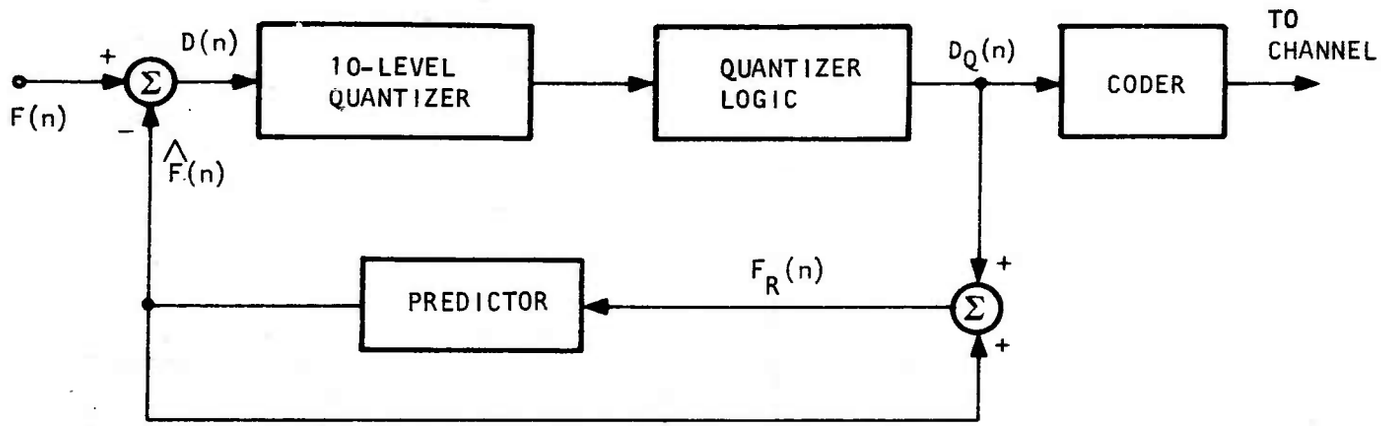


(a) ORIGINAL SYNC SIGNAL

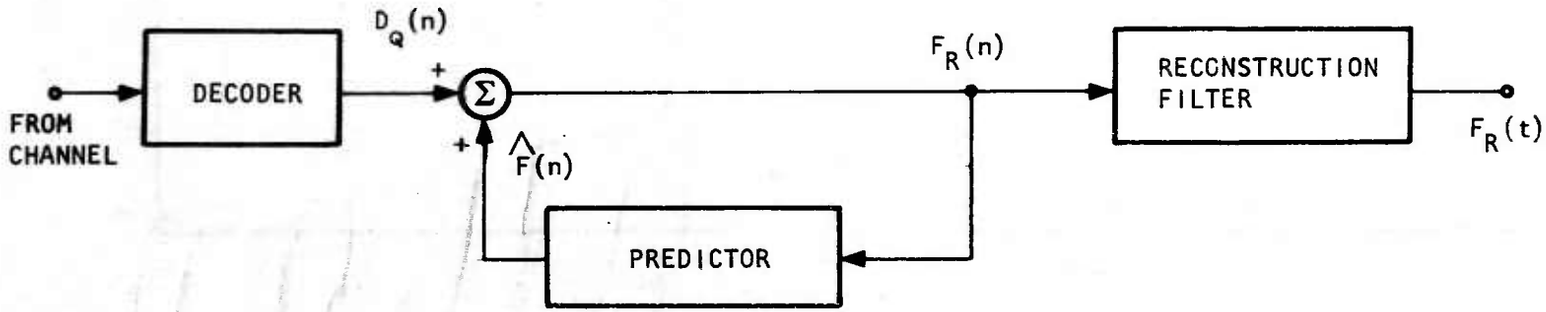


(b) CODED SYNC SIGNAL

Figure A-15. Computer Simulation of Coding of Horizontal Sync Signal by 3-Bit, -10 MHz (Two-Thirds Nyquist) DPCM Coding System



(a) TRANSMITTER UNIT



(b) RECEIVER UNIT

Figure A-16. Dual-Mode DPCM/Deltamodulation Image Coder

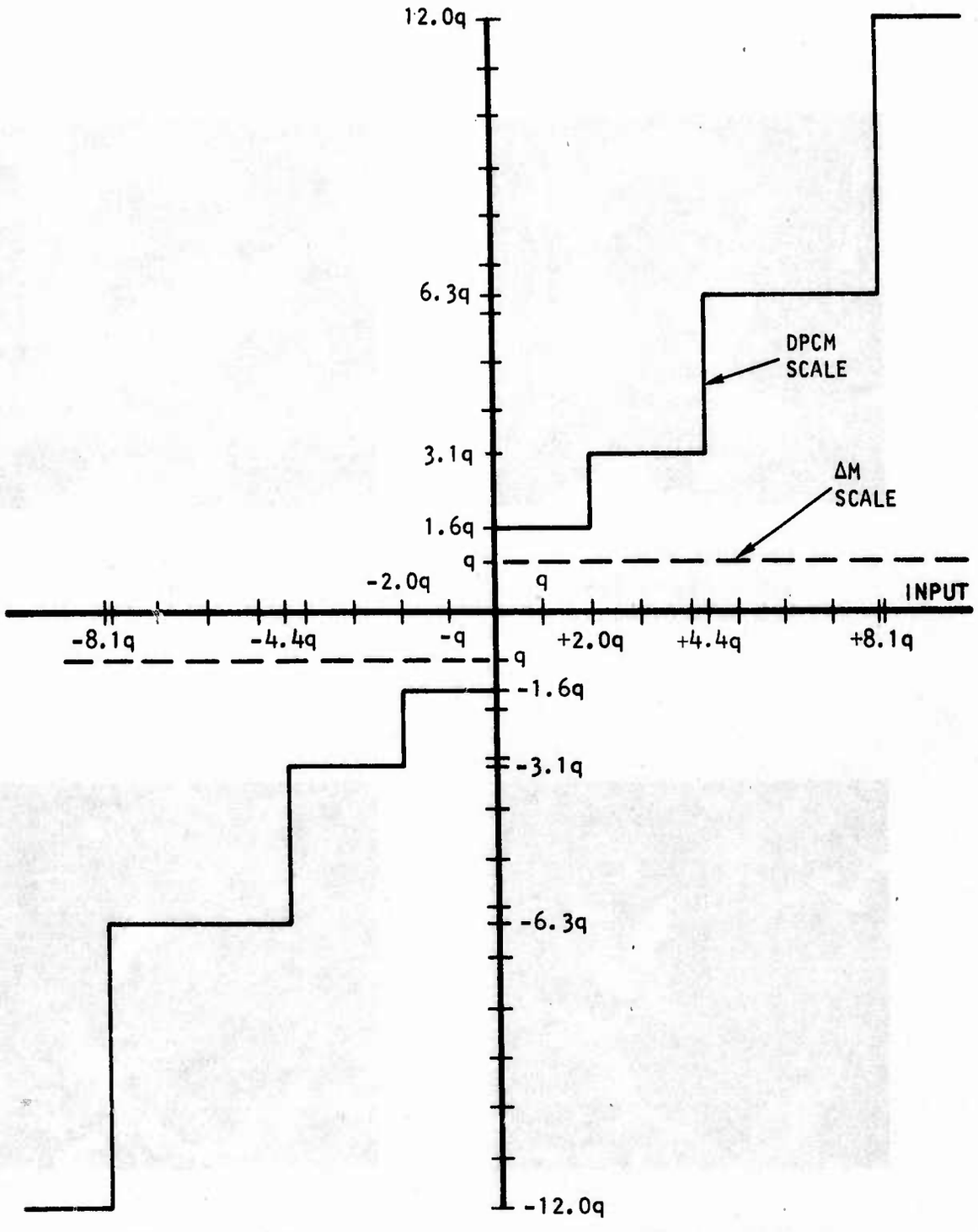
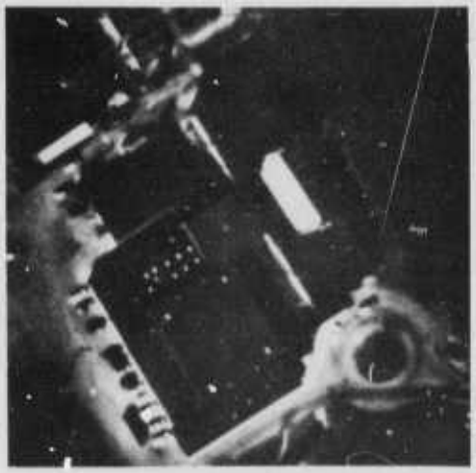


Figure A-17. Quantizer Scale for Dual-Mode Coder

a. ORIGINAL PCM
256 x 256 PIXELS
8.0 BITS/PIXEL

b. DUAL MODE CODED,
2.0 BITS/PIXEL



c. ORIGINAL PCM
512 x 512 PIXELS
8.0 BITS/PIXEL

d. DUAL MODE CODED
2.0 BITS/PIXEL

Figure A-18. Computer Simulation of Basic Dual Mode DPCM/Delta-modulation Image Coding System.

is operating in the delta mode, the difference signal is quantized to a positive or negative reconstruction level based upon the polarity of the difference signal. In the DPCM mode, the difference signal is quantized to one of eight levels according to the tapered quantization scale. The appropriate quantized difference signal (two-level or eight-level) is fed back to the predictor by the quantizer logic circuit. The coder performs the assignment of code bits given in Table A-2. The DPCM code is a reflected gray code.

The switching logic implemented by the quantizer logic circuit is quite simple. If the coder is in the delta mode and three consecutive +q reconstruction levels or three consequentive -q reconstruction levels occur, the coder switches to the DPCM state. If the coder is in the DPCM mode and the quantized difference changes from the -Q to the +Q reconstruction levels, or vice versa, an idling condition is said to occur, and the coder switches to deltamodulation. The switching logic is based completely on the past history of the quantized reconstruction levels, which are uniquely related to the transmitted code bits. Thus, the receiver can determine when to switch modes by examination of the transmitted code bits. If the receiver is in the delta mode and the last three received code bits are (0. 0, 0) or (1, 1, 1), the mode switches to DPCM. Conversely, if the receiver is in the DPCM mode and the last six code bits are (0, 0, 0, 1, 1, 1) or (1, 1, 1, 0, 0, 0), the mode switches to deltamodulation. Photographs of images coded by the basic dual-mode coder are shown in Figure A-18. In this simulation,

TABLE A-2. BASIC DUAL-MODE CODER CODE ASSIGNMENT

Delta Mode		DPCM Mode	
Quantization Level	Code	Quantization Level	Code
+q	1	Q	1 0 1
-q	0	Q	1 0 0
		Q	1 1 0
		Q	1 1 1
		-Q	0 0 0
		-Q	0 0 1
		-Q	0 1 1
		-Q	0 1 0

the quantization levels have been selected so that the coder remained in each mode equally to obtain an average coding of about 2.0 bits/pixel. There is no apparent granularity in the reconstructed image, but an annoying serration along sharp edges is apparent. This jaggedness occurs because the delay in detecting a sharp brightness transition from delta to DPCM may vary from one to three pixel periods for nonvertical steep brightness transitions.

4.2 OVERSAMPLED DUAL-MODE CODER

The dual-mode coder developed by Frei, Velliger, and Schindler avoids the problem of jagged edges of sampling the video signal at three times the normal rate and determining if a brightness change has occurred from these samples. For notational purposes, samples obtained by sampling at the Nyquist rate are called Nyquist samples, and samples obtained by sampling at three times the Nyquist rate are called super Nyquist samples. The oversampled dual-mode coder also is indicated by Figure A-16 when assuming that F(n) represents super Nyquist samples. The quantizer logic is as follows. If the coder is in the delta mode and the reconstruction levels of three successive super Nyquist samples are (+q, +q, +q) or (-q, -q, -q), the coder switches to DPCM and operates at the Nyquist rate in DPCM. If the coder is in the DPCM mode and the reconstruction levels for two successive Nyquist samples are (+Q , -Q) or (-Q , +Q), the coder switches state to deltamodulation.

The DPCM code for the oversampled dual-mode coder is the same as that for the basic dual-mode coder. The delta mode transmission code is given in Table A-3. When the coder is in the delta mode, the three quantized differences of the super Nyquist samples are examined together. If two of the three quantized differences are positive and the third is negative, a one-bit is transmitted. Conversely, a zero-bit is transmitted if two of the differences are negative and the third is positive. If all three differences are positive, the code is (1 1 1 1 0); the last two bits are marker bits inserted to prevent ambiguity. The marker bits are necessary because a long sequence of delta one-code bits may be encountered. After three ones of such a sequence, a zero-bit is inserted in the sequence. A sequence of three negative delta differences is coded by (0 0 0 0 1), where the last two bits are marker bits to distinguish this code from a long sequence of delta zero-bits. After three delta zeros, a one-bit is inserted as a marker.

With this coding logic, the receiver can unambiguously decode the received bit stream and determine when to switch states. The logic of the receiver decoder is summarized in Table A-4. The decoder stores the previous six bits received (C1 to C6), where C6 is the more recent bit. The first two rows of the table indicate the DPCM idling condition (-Q to +Q) or (+Q to -Q) and signal a switch to the delta mode for subsequent operation. The third and fourth rows contain the codes that indicate that the delta quantizer produced the quantized differences (-q, -q, -q) or (+q, +q, +q). The appropriate action is to discard the marker bits C4 and C5 and to regard bits C1, C2, C3 as the DPCM code for a reconstructed pixel difference. Finally, the last two rows contain three delta code bits C1, C2, C3 and an appended marker bit C4. The marker bit is discarded, and bits C1, C2 and C3 are decoded as delta bits. Computer simulation photographs of images coded by the oversampled dual-mode coder are given in Figure A-19. The results are quite good, with no apparent jaggedness in the vicinity of sharp brightness transitions.

a. ORIGINAL PCM 256 x 256
PIXELS, 8.0 BITS/PIXEL

b. DUAL MODE CODED
2.0 BITS/PIXEL

c. ORIGINAL PCM
512 x 512 PIXELS
8.0 BITS/PIXEL

d. DUAL MODE CODED
2.0 BITS/PIXEL

Figure A-19. Computer Simulation of Oversampled Dual Mode DPCM/Deltamodulation Image Coding System

TABLE A-3. OVERSAMPLED DUAL-MODE CODER DELTA MODE TRANSMISSION CODE

Delta Reconstruction Levels, Super Nyquist Sample No.			Code
1	2	3	
+q	+q	+q	1 1 1 1*0*
+q	+q	-q	1
+q	-q	+q	1
-q	+q	+q	1
-q	-q	+q	0
-q	+q	-q	0
+q	-q	-q	0
-q	-q	-q	0 0 0 0*1*

*Marker bits

TABLE A-4. OVERSAMPLED DUAL-MODE CODER DECODER LOGIC

State	Bit No.						Action
	C_1	C_2	C_3	C_4	C_5	C_6	
DPCM	0	0	0	1	1	1	Switch to delta
DPCM	1	1	1	0	0	0	Switch to delta
Delta	0	0	0	0	1	X	Switch to DPCM and discard C_4 and C_5
Delta	1	1	1	1	0	X	Switch to DPCM and discard C_4 and C_5
Delta	0	0	0	1	X	X	Discard C_4
Delta	1	1	1	0	X	X	Discard C_5

5. SUMMARY

On the basis of coding fidelity and practicality of implementation, the review of potential techniques for digitally coded television signals for transmission over a time multiplex communication link shows that the best candidate systems for image coding at a design rate of 2.0 bits/pixel or lower are the family of linear predictive image coding systems. A detailed study of linear predictive image coding systems indicated that the following systems satisfy the design requirements:

(a) Eight-level DPCM coder with video sampling at two-thirds the Nyquist rate

(b) Set of three or more eight-level DPCM coders with time multiplexing of DPCM difference signals

(c) Oversampled dual-mode DPCM/deltamodulation coder

The system listed in a above is advantageous because of its simplicity, but it causes some loss in horizontal resolution. That for b is quite attractive for the transmission of multiple television channels because it provides almost the same quality as 3.0 bits/pixel DPCM for each channel at very little extra coder complexity as compared to a set of independent DPCM coding systems. The system in c results in very good quality coding at 2.0 bits/pixel for one or more channels. However, the system is complex and requires buffer storage.

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APPENDIX B

BIDIRECTIONAL DIGITAL DATA LINK DEVELOPMENT

APPENDIX B

BIDIRECTIONAL DIGITAL DATA LINK DEVELOPMENT

1. INTRODUCTION AND SUMMARY

This appendix presents the results of investigations performed for Eglin AFB by AiResearch resulting in development of a data transmission link capable of sending digital code voltage pulse waveforms in opposite directions simultaneously along one coaxial transmission line. Time sharing or synchronizing between the signals in the two directions of transmission is not necessary, and interference from oppositely directed digital code signals on the received signal at each end is acceptably low. Studies indicate that two systems are particularly adaptable to the high data rates required, one system using coaxial line directional couplers and the other transformer hybrid junctions.

The hybrid junctions were used to fabricate a high-bit-rate, full-duplex data link that was successfully demonstrated. At bit rates up to 200 megabits/sec over a coaxial transmission line length equivalent of up to 300 ft of RG-14U cable, signal-to-noise ratios of greater than 10 to 1 for received signals over oppositely directed transmissions were demonstrated. While this hardware system was chosen for a two-station, point-to-point, high-bit-rate requirement, the AiResearch investigations indicate that practical design of multiple-station, lower-bit-rate, direction-selective multiplex bus systems may be feasible using the directional couplers alone, or in combination with the hybrid junctions.

Further investigation in some areas is needed, including sources for small devices with higher isolation or directivity having bandwidths extending to frequencies below 1 MHz. System performance as affected by environment and by practical field-use limits of transmission line system and coupler impedance variability should be evaluated.

2. SYSTEM REQUIREMENTS

From the requirements set forth in the initial Multiport Multiplex Group statement of work and subsequent discussions with Eglin AFB/Air Force Armament Laboratory personnel, the basic digital data transmission link requirements were developed as follows:

- Transmission of pulse-waveform digital data at rates up to 200 megabits/sec.
- Simultaneous transmission and reception of data pulse trains in both directions along the same transmission line, asynchronously, with better than 10-to-1 amplitude ratio between signal received at either end and interference from the adjacent signal being transmitted in the opposite direction.

- Link to be any length up to 300 ft, with no adjustment or tuning required to accommodate any particular length and no repeaters in the line.

- Transmission line must be a standard RG/U type proven acceptable for USAF flight application and double-shielded to minimize EMI effects with 1/2-in -dia maximum approximate to conserve space and weight.

3. DIGITAL DATA RATE - TRANSMISSION LINE LOSS RELATIONSHIP

The ability to detect unambiguously the sequential relationships of short pulses transmitted down the 300-ft maximum-length transmission line is partly dependent on the extent of pulse waveform degradation and overlap as the pulses reach the receiving terminal. A preliminary evaluation of these factors was performed utilizing an analytical transient response method developed by Dr. H. F. Taylor, Naval Electronics Laboratory Center, San Diego, based on expressions from R. E. Matick's text Transmission Lines for Digital and Communication Networks (McGraw-Hill, 1969). In this approach, the effects of transmission line attenuation constant and length are evaluated. The transmission line transfer function is driven by a unit impulse input (essentially zero width and infinite height unit area). From the transmission line transfer function response to this input, the maximum bit rate is assumed to exist when two adjacent pulses overlap at the 10 percent of maximum amplitude points. This maximum bit rate is defined as the inverse of the calculated time width of a single received pulse as measured between the 10 percent of maximum amplitude points on the leading and trailing edges of the pulse.

Within the assumptions of this analysis, a guideline value was derived for tolerable transmission line loss to handle a maximum 200-megabit/sec pulse transmission rate over a 300-ft line span. For the frequency range where transmission line loss is determined primarily by skin effect (loss proportional to square root of frequency), the following relationship was utilized.

$$\alpha/f^{1/2} = \left(\frac{4\pi}{L^2 \times 7.8 \times \text{Bit Rate}} \right)^{1/2}$$

$$= \left(\frac{4\pi}{91.44^2 \times 7.8 \times 2 \times 10^8} \right)^{1/2}$$

$$= 9.815 \times 10^7$$

where α = transmission line attenuation constant in nepers/meter

f = radio frequency in Hz at which α is measured

L = transmission line length in meters (300 ft = 91.44m)

7.8 = factor relating pulse width at the 10 percent amplitude levels

Using this approach, the value of $\alpha/f^{1/2}$ (constant ratio below frequencies where dielectric losses become significant) at the 200 megabit/sec data rate upper limit is 9.815×10^{7}. At f = 100 MHz, α = 0.0098 nepers/meter, or 2.59 db/100 ft. At 200 MHz, the attenuation is 0.0139 nepers/meter, or 3.67 db/100 ft. Given these tentative criteria for maximum permissible transmission line loss, potentially applicable double-shielded transmission lines qualified for USAF airborne environment were surveyed. Representative types and some of their characteristics are listed in Table B-1. The low attenuation values associated with RG-14A/U line were utilized in this investigation.

4. DATA PULSE GENERATION AND MONITORING

To permit experimental examination of transmission lines and potential duplexing schemes, it was first necessary to obtain equipment capable of generating and displaying short sequences of pulse waveforms at 200-megabit maximum repetition rates (5-nsec data window). To meet the system requirement for operation without tuning adjustments required for any desired length of transmission line, it was necessary that the test equipment always allow termination of the lines at the characteristic line impedance value to minimize reflections, thus allowing flat (nonresonant) line operation over any length.

TABLE B-1. RG/U MIL-TYPE, DOUBLE-SHIELDED TRANSMISSION LINE (50-OHM COAS, 95-OHM TWINAX)

RG-/U Number	Diameter, in.	Attenuation, db/100 ft		
		100 MHz	200 MHz	300 MHz
9B	0.420	2.1	3.0	4.5
14A	0.545	1.4	2.0	3.1
94A	0.470	1.7	2.5	3.5
115	0.375	2.0	2.9	4.2
116	0.475	2.1	3.0	4.5
225	0.430	2.1	3.0	4.5
226	0.500	1.7	2.5	3.5
111 amp 95 ohm TWINAX	0.470	3.0	4.5	6.8

Initially, the very short pulses associated with the maximum data rate were generated repetitively by charging a short length of coaxial line to a dc potential and then discharging into the transmission line link (of the same impedance as the charged line) via a coaxially mounted, mercury-wetted (no contact bounce) reed relay. At the receiving end, the line was terminated by a resistance matching the low line impedance and shunted by the high impedance input to a sampling oscilloscope (capable of gigaHz response to a repetitive function.) An alternate employed was a Tektronix Model 454 oscilloscope photographed with high-speed Polaroid® film.

Since use of this equipment resulted in time-consuming and cumbersome data recording, a survey was made of existing high-frequency-response equipment. Two instruments were chosen. To satisfy the digital pulse simulation requirement, a Datapulse Model 113 B, with the capability of delivering pulses as short as several nsec in duration, and a 50-ohm generator output impedance to match the transmission line was used. Also, the Model 113 has provisions for controlled gating of groups of one or more pulses at any desired pulse-group repetition rate. This feature permits evaluation of pulse-to-pulse interaction and pulse train dc level wander as a function of pulse train length. For the receiving end, the Tektronix Model 7904 oscilloscope, providing 500-MHz-bandwidth and a 50-ohm input impedance to match the transmission line, was chosen. Horizontal sweep rates of sub nsec/cm provides quite adequate pulse waveform display capability. Availability of equipment, in combination with standard peripheral instruments, allowed the data link evaluation to proceed expeditiously with correct impedance matching at input and output interfaces.

5. BIDIRECTIONAL TRANSMISSION TECHNIQUE SURVEY

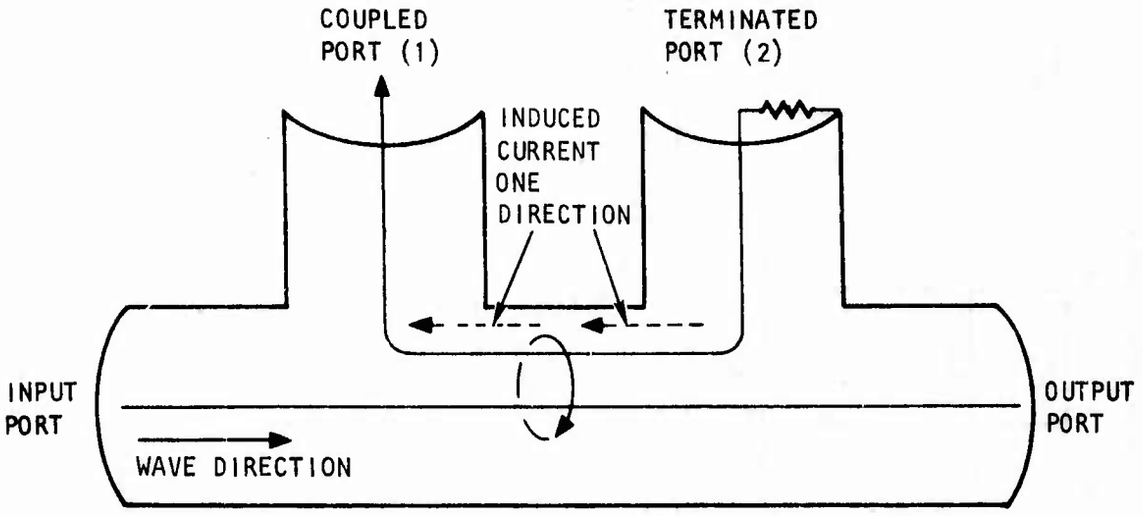
To take advantage of any recent work relating to high data rate duplexing, a literature search was conducted at the technical libraries at AiResearch, UCLA, and USC. Among a number of approaches published on simultaneous two-way data transmission, only one was found that appeared applicable to the required hundred megabit data range . A twin-conductor coaxial-type transmission line (such as RG-111A/U) is used. In this twin-line method, duplexing was accomplished by transmitting in one direction through the two inner conductors, driving one against the other. Independent reverse direction transmission was accomplished by driving both center conductors at the same potential against the surrounding shielding. Evaluation of the twinax method showed that the risk against making a practical system in the time available was too great. Two other duplexing possibilities were proposed by AiResearch for further investigation, both utilizing single coaxial conductor transmission line. The first one studied was based on use of coaxial line type directional couplers, and the second on transformer hybrid junction devices. These are discussed in the following paragraphs.

1. H. Guckel, "A Wide-Band Simultaneous Send-Receive Circuit for Data Cables," Proc. IEEEE, Vol. 60, pp. 643-4, May 1972.

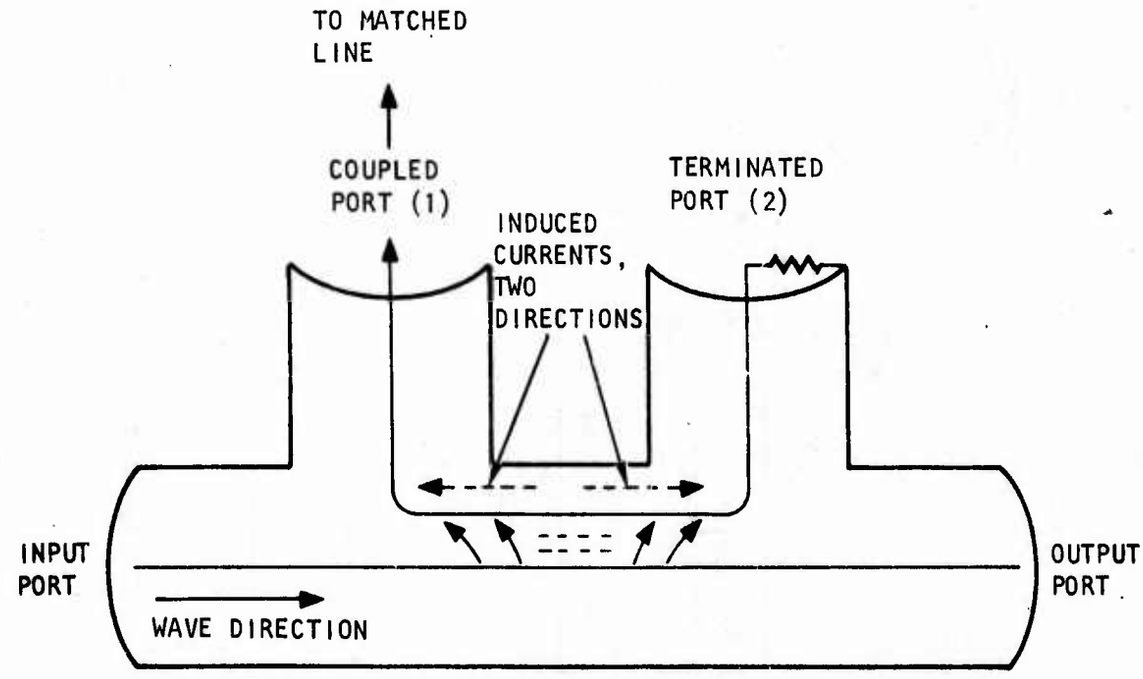
6. DUPLEX LINK UTILIZING COAX LINE DIRECTIONAL COUPLERS

As one of the two most promising duplex link approaches, utilization of the properties of coaxial line directional couplers was investigated at AiResearch. The applicable feature of these couplers is that when connected in series with a coaxial line transmission link, they will couple out energy through a third port much more readily for one direction of wave travel through the line than for waves travelling simultaneously in the opposite directions down the same line. An example of a physical mechanism with the above characteristics-- a simplified broad-band, loop-type directional coupler-- is shown in Figure B-1. Such directional couplers form a class of transmission line systems in which a secondary line couples to a primary line to extract a portion of the energy from the wave travelling along the primary line in one direction, while discriminating against coupling to an oppositely directed wave on the primary line. Figure B-1A shows a transverse electromagnetic wave travelling left to right in the primary line, with the magnetic flux lines threading the loop formed by the secondary line center conductor. The induced wave current travels only in one direction in the loop. At the same time (as illustrated in Figure B-1), the electric field from the same primary line wave induces two opposite currents in the secondary loop. By tailoring the loop geometry, the coupling effects can be made equal, so the power coupled to port 2 (terminated with the characteristic line impedance) is made nearly zero by 180-deg phase difference between the two current components induced by the electric field and by the magnetic field. A wave is coupled to port 1 (coupled port) because the current components induced by the two fields are in phase. For right-to-left wave travel in the primary line, the magnetic coupling phase relationship is reversed, resulting in very small coupling to port 1, and a wave is induced in port 2 where it is dissipated without reflection in the matched resistive termination.

The ratio of power induced in the coupled port to power at the input port is the coupling of the directional coupler, and for this application a commonly available coupling value of -10 db could be utilized. The directivity of the coupler is the ratio of intentionally coupled power out of the coupled port to undesired power measured at this same port when a wave of fixed power travels first in the desired direction and then in the opposite direction (fed into the output port). Couplers with 30-db directivity are readily available. The isolation in a directional coupler is the ratio of undesired power induced in the coupled port to the inducing primary line power travelling in the uncoupled direction. This is not ordinarily specified, but is the sum of the coupling and the directivity, or about 40 db for many available couplers. As shown subsequently, the difference in db between the isolation and the coupling for a particular directional coupler is a primary determiner of achievable signal-to-noise ratio in a bidirectional transmission link. These directional coupler characteristics can be utilized for bidirectional transmission of digital pulse data in the configuration shown schematically in Figure B-2. Two directional couplers designed for 50-ohm line operation are connected , input port to input port, by up to 300 ft of coaxial line (double-shielded, 50-ohm RG-14A/U in this example). One pulse transmitter (50-ohm output impedance) is connected to each coupler output terminal, and one receiver (50-ohm input impedance) is connected



(a) MAGNETIC COUPLING



(b) ELECTRIC FIELD COUPLING

Figure B-1. Loop Type Directional Coupler

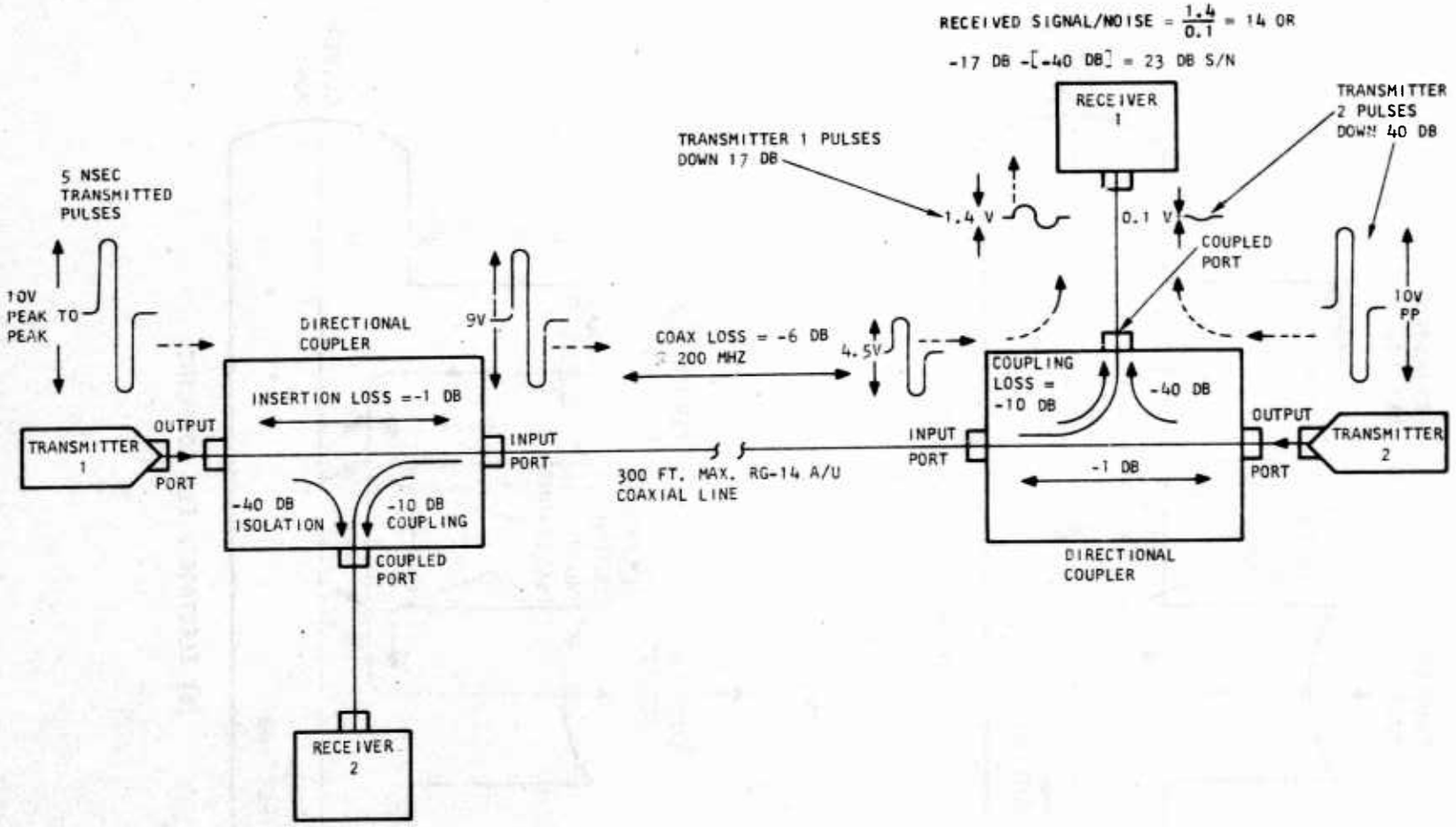


Figure B-2. Directional Coupler, Full Duplex Data Link

to each coupled port. With all impedances properly matched, signal reflections are minimized and a nonresonant system exists which is insensitive to transmission line length (except for signal loss proportional to length).

To demonstrate the bidirectional operation, a bipolar pulse signal transmission is traced from left to right (bipolar waveform used to avoid dc wander in an ac coupled system). Starting at the first transmitter (XMTR 1), a bipolar pulse of 10 v peak-to-peak amplitude (much higher amplitudes can be used) is generated by one of the techniques discussed in para 9 and transmitted through the coupler, entering the RG-14A/U transmission line 1 db down (coupler insertion loss) with an amplitude of 9 v peak-to-peak. Propagating along the line to the right, the pulse passes into the right-hand coupler input port, attenuated through the 300-ft transmission line by another 6 db to 4.5 v peak-to-peak. This 6-db loss is approximate and is based upon a 200-MHz sinusoidal wave signal loss of 2 db/100 ft measured for the RG-14A/U, whereas the amplitude-vs-frequency spectral distribution for a random number digital pulse signal can be quite broad and is dependent upon specific pulse code format. This 200-MHz loss agrees closely with attenuation observed for the 5-nsec bipolar pulse waveforms generated from the Datapulse 113.

Inside the right-hand coupler, the signal is split two ways. One component passes straight through the coupler, attenuated by 1 db, and is dissipated in the 50 ohm resistive impedance of the second transmitter (XMTR 2). The other component couples through the output port, attenuated by an additional 10 db to a value of 1.4 v peak-to-peak, and is fed into the left-to-right receiver (RCVR 1) 50-ohm input. At the same time, an interfering signal generated by the right-to-left transmitter (XMTR 2) also couples from the output port to RCVR 1. However, this interfering signal component from XMTR 2 is attenuated by the 40-db isolation action of the coupler to a level of 0.1 v peak-to-peak, assuming the output amplitudes of pulses from both XMTR 1 and XMTR 2 are 10 v peak-to-peak. Thus, the left-to-right receiver sees the desired signal at amplitude 1.4 v peak-to-peak and the interfering signal at amplitude 0.1 v peak-to-peak. The signal-to-noise ratio resulting from summing these two signals at the receiver input is 1.4/0.1, or 14 to 1, corresponding to about 23 db. This agrees with the difference between the -17 db transmission losses sustained by the XMTR 1 signal (-1 db coupler insertion, -6 db coaxial line loss, -10 db coupling factor) and the interfering signal -40 db isolation attenuation through the coupler. The right-to-left signal transmission sequence from XMTR 2 to RCVR 2 is the mirror image of the path from XMTR 1 to RCVR 1, and results in the same signal-to-noise ratio for simultaneous two-way transmission. This 14-to-1 ratio provides a margin for additional degradation in a practical data link, such as from pulse position jitter and less-than-perfect impedance matching. A 2-watt line-driving pulse transmitter would deliver bipolar code pulses into a matched 50-ohm load at the receiver with a signal level of 4.0 v peak-to-peak, which should prove quite adequate for further digital processing. At an input power level of 5 watts, which can be handled by some of the small (1.3 in. by 1.3 in. by 0.75 in.) 10-db couplers available, a received signal level of 6.3 v peak-to-peak could be obtained.

An alternate approach proposed by AiResearch to the directional coupler system outlined above would utilize transformer hybrid junctions. These junction devices can perform signal coupling and isolation functions in a bidirectional data link, providing system performance comparable to that obtained with directional couplers. The directional couplers, as discussed earlier in this section, may be better adapted to a multi-station bus-oriented duplexing system (lower in-line insertion loss, i.e., 1 db vs 3.5 db) than the junction devices. However, for the two-station, point-to-point, high-data-rate system required for wide band video digital transmission, investigations showed that the hybrid junctions would provide satisfactory duplex performance at lower cost and smaller size than the directional couplers. Therefore, the alternate approach was chosen for hardware implementation as discussed in the following paragraph.

7. TRANSFORMER HYBRID JUNCTION DUPLEX LINK DEVELOPMENT AND TEST

Duplexer investigations showed that use could be made of a class of rugged, compact (1/8 in. by 3/8 in. by 1/2 in. flatpack), inexpensive (10 to 50 dollars per unit) transformer hybrid junction power divider (ferrite core) devices. Features that make these hybrid junction dividers applicable to design of a duplexing link are:

- A signal from a transmission line into the junction symmetric input (summing) port will divide and couple pulse signal power equally (3.5 db down, including insertion losses) to two other output ports.
- A pulse signal transmitted back into the divider from either of the above two divider output ports will couple a signal to the input port about 3.5 db down from the original signal amplitude, but will couple to the other output port a signal amplitude down by as much as 40 db or more (0.01 of input signal amplitude isolation). Power not coupled out is dissipated in the internal junction terminating resistor (0.05 watts maximum internal dissipation for the flatpacks).
- The three ports each present a true 50-ohm resistive match to any 50-ohm resistive load, including transmission line of 50-ohm characteristic impedance, resulting in a nonresonant system almost free from internal reflections.

(See para 8 for a description of the hybrid junction operating principles.) These characteristics are analogous to those of the directional couplers, and are equally applicable to bidirectional signal transmission.

A functional schematic of the hybrid junction duplex data link that was successfully demonstrated at AiResearch is shown in Figure B-3. Starting at XMTR 1 transformer (50-ohm source impedance), a sequence of 1-v peak-to-peak, 5-nsec pulses (bipolar to avoid dc wander) simulating a digital data stream is coupled through coax line into port A of the hybrid junction power divider. The signal splits, attenuated by 36 db (for the particular dividers used) at the opposite port B, and 3.5 db at the symmetric port C (3-db coupling, 0.5-db insertion loss). The 0.67-v peak-to-peak signal from port C is fed into the

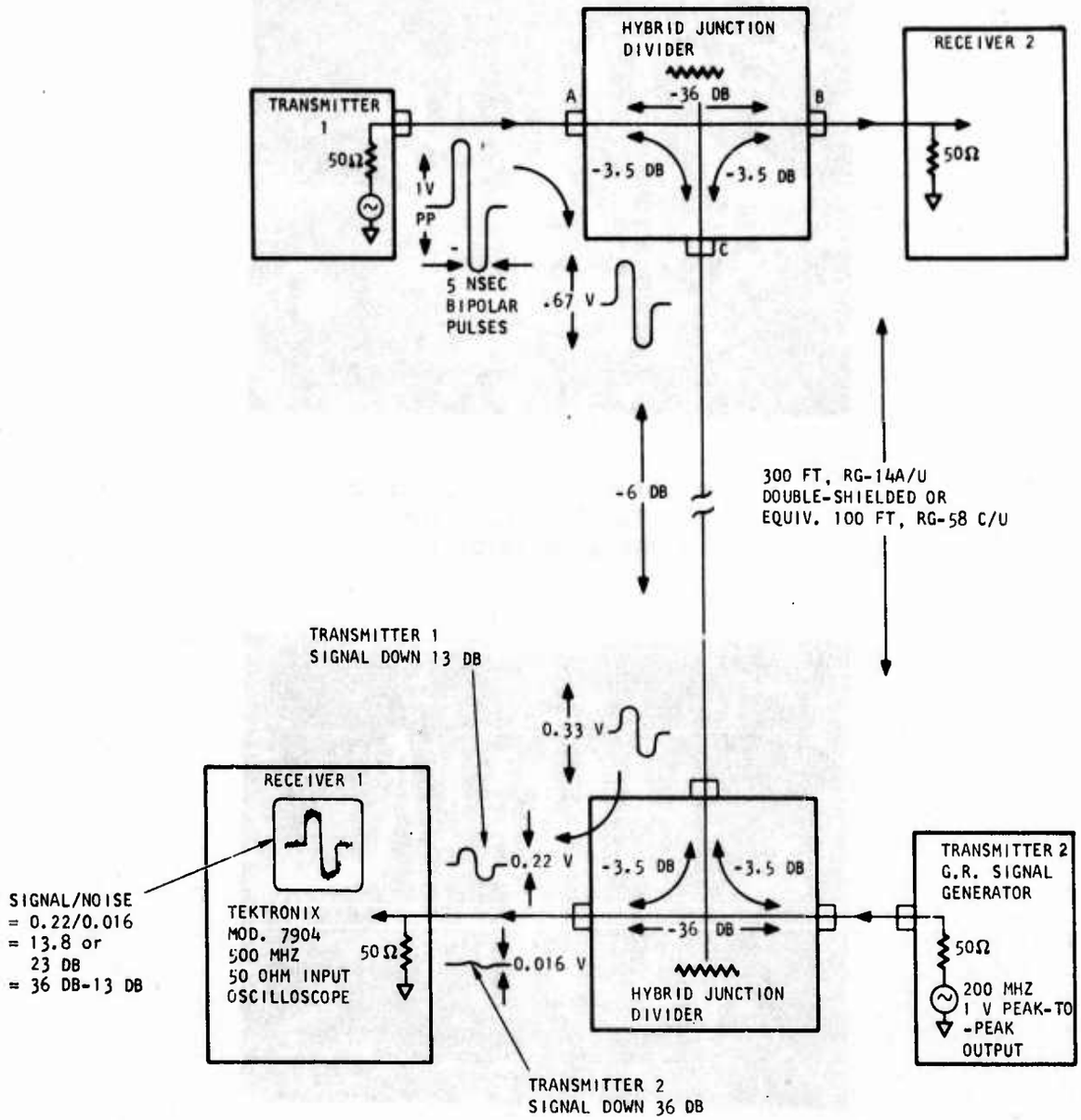
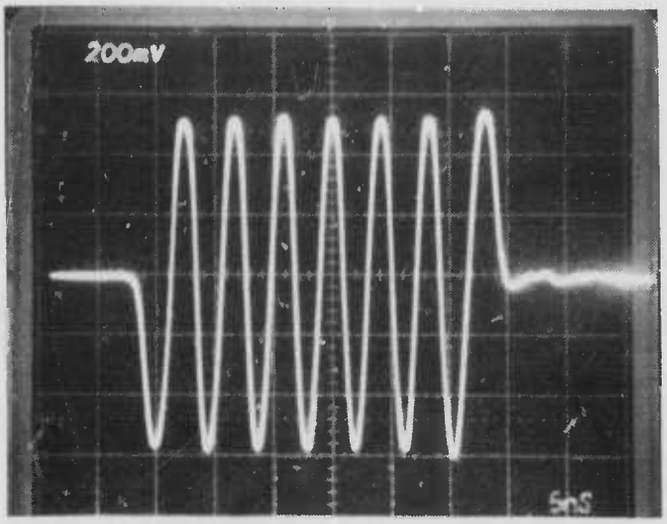
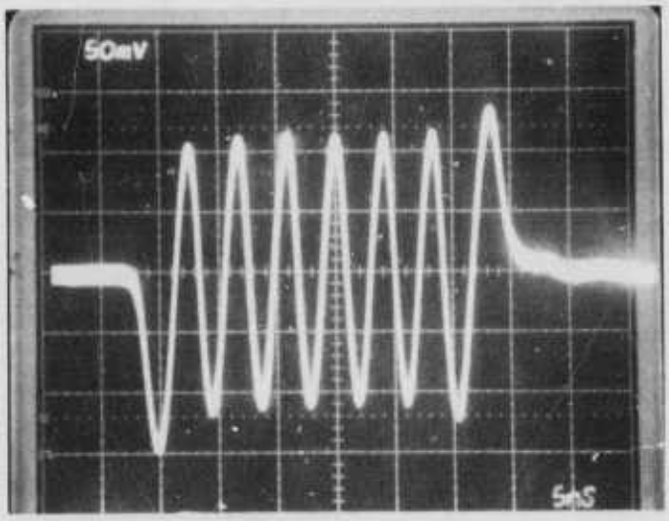


Figure B-3. Hybrid Junction Duplex Link



(a) TRAIN OF 200 MEGABIT/SEC BIPOLAR PULSES, DUPLEX DATA LINK INPUT 1.



(b) DUPLEX DATA LINK OUTPUT 1, AFTER TRANSMISSION VIA EQUIVALENT OF 300 FT RG-14A/U COAX. ADJACENT XMTR INTERFERENCE -23 DB.

Figure B-4. Simultaneous Bidirectional 200 Megabit/Sec Data Link Transmission

data link transmission line. In this demonstration link, the 300 ft (maximum) equivalent of RG-14A/U was provided for convenience by 100 ft of RG-58C/U, both lengths having the same 6-db loss at 200 MHz.

At the far end of the transmission line, the pulse amplitude is down to 0.33 v peak-to-peak attenuated by the 6-db line loss. This signal is fed into the symmetric port of a second junction divider and divides equally to each of the two other ports, attenuated by 3.5 db to a level of 0.22 v peak-to-peak. The signal power component coupled into transformer 2 is dissipated without reflection in the matched 50-ohm generator impedance. The other output port signal of 0.22 v peak-to-peak is coupled into the matched 50-ohm input of the Tektronix 7904 oscilloscope. Also received at the oscilloscope is an interfering signal generated by transformer 2, which is transmitting at the same level as transformer 1 back to receiver 2 through a signal path totally symmetrical to the transformer 1 path. The heart of the duplex operation lies in the isolation provided by the junction between the transformer 2 port and the receiver 1 port (and the same at the other end of the link between transformer 1 and receiver 2). The particular couplers utilized in this test link have an isolation value of 36 db, which attenuates the 1-v peak-to-peak transformer 2 signal to 0.016 v peak-to-peak at the oscilloscope input. The reverse direction transmission signal from transformer 2 is simulated by a General Radio Model 1021-A cw signal generator with a PI tuner.

Thus, the signal-to-noise ratio for the digital data stream at receiver 1 is 0.22/0.016 = 14, or 23 db, which is very adequate for unambiguous digital data recovery. The transformer 2 signal can be traced back to the receiver 2 position to show the same 14:1 signal-to-noise ratio, but now favoring the transformer 2 signal as received. This constitutes a full duplex data link.

Actual performance of the hybrid junction duplex link as described is shown in Figure B-4. Figure B-4a shows a train of 5-nsec bipolar pulses as coupled into the data link at transformer 1. Figure B-4b shows the same pulse train as received at receiver 1 through the equivalent of 300 ft of RG-14A/U coaxial cable and with an adjacent, nonsynchronized transmitter coupled into the system and tuned near 200 MHz to produce maximum interference at receiver 1. A photograph of the full duplex data link test configuration is shown in Figure B-5.

While the 14:1 signal-to-noise ratio obtained is more than satisfactory for data recovery, a higher signal level at the output is desirable for direct digital data processing. The 0.22 v peak-to-peak signal recovered in the above demonstration link was dictated by the maximum output value of 1 v peak-to-peak obtainable from the General Radio 200-MHz signal generator (transformer 2), which required a matching level of 1 v peak-to-peak to be set on the pulse generator (transformer 1) output. The bipolar input pulse amplitude to the internally terminated hybrid flatpacks can be raised to about 6.6 v peak-to-peak without exceeding the 0.05-watt limit on internal power dissipation. This would provide a 1.4 v peak-to-peak data link system output level and 0.11-watt average pulse power input at each transmitter. Four-port hybrid junctions (para. 8) can have the fourth port terminated with a higher wattage external resistor, and the small flatpacks can then handle 1-watt average pulse

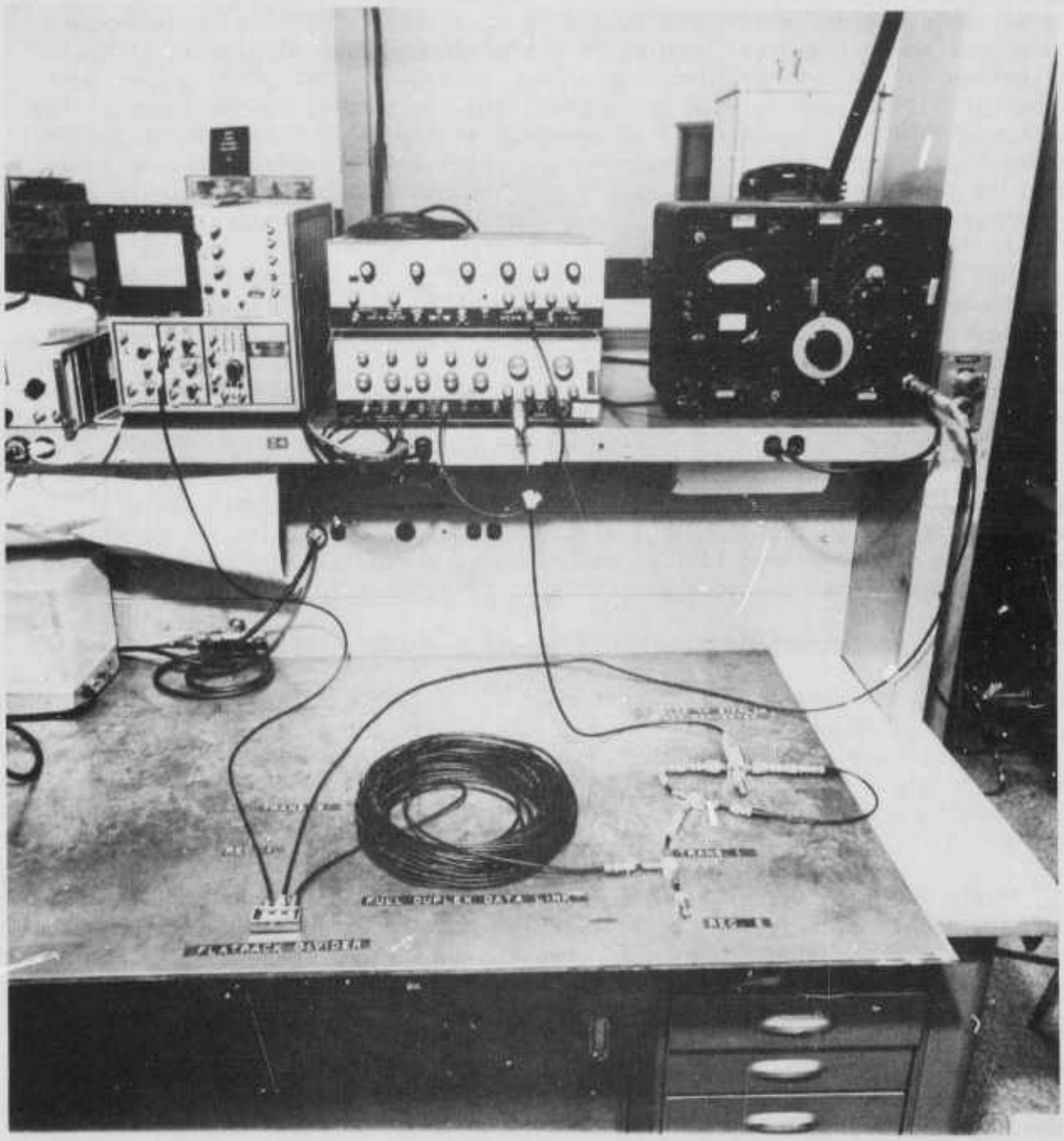


Figure B-5. Bench Test Configuration for Full Duplex Digital Data Link

power input. This translates to about 4.5 v peak-to-peak pulse signal output. Slightly larger stripline-mount 4-port packages can handle up to 5-watt average input power.

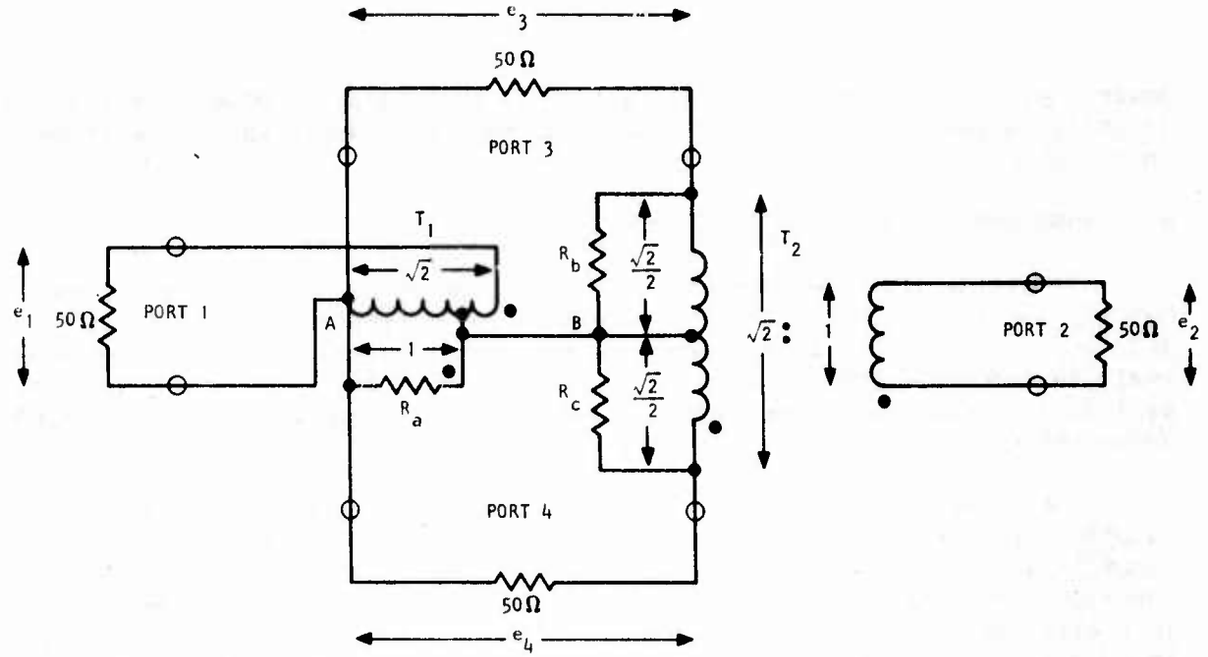
8. TRANSFORMER HYBRID JUNCTION OPERATING PRINCIPLES

All of the divider-summer-phase inverter devices used are transformer hybrid junctions. These devices are available in very compact (1/8 in. by 3/32 in. by 1/2 in.) flatpack versions for stripline mounting. They contain small ferrite core transformers (core size approximately 1/8 in. by 3/32 in. by 3/32 in.) wound with few turns (low magnetizing inductance, yielding good pulse response).

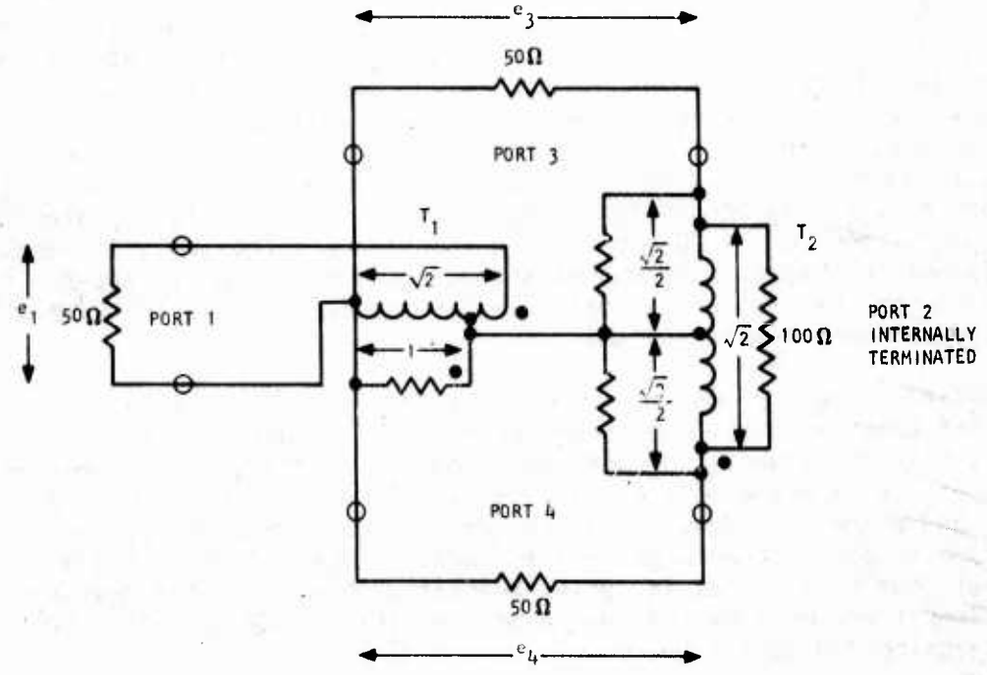
Simplified schematics are shown in Figure B-6 to demonstrate how the junctions perform their functions. A full four-port transformer hybrid junction with ideal transformers is shown in Figure B-6a. In this case, the junction is designed to match to a 50-ohm resistive load at each port, compatible with use of 50-ohm coaxial transmission line for data link application. The junction characteristics of value in the duplexing application can be analyzed by applying a signal into each of the four inputs shown in Figure B-6a, one at a time. Power applied to port 1 couples through the impedance-matching autotransformer T_1 to the center-tapped winding of T_2. Here, the power divides equally, and equal currents flow in opposite directions through the two halves of the tapped winding into the 50-ohm external resistive loads at ports 3 and 4. There is an equal power split (-3 db) between ports 3 and 4, and 0 deg phase shift from e_1 to e_3 and e_4. The equal and opposite currents in the tapped T_2 winding produce no coupling across T_2, so e_2 is zero and port 2 is isolated from port 1. The port 3 and port 4 50-ohm load resistors are effectively in parallel, producing a 25-ohm resistance (dotted resistance R_a) across the T_1 tapped winding, and this 25-ohm resistance is transformed by the T_2 turns ratio $(2^{1}/2/1)^2$ to match the 50-ohm port 1 external source.

Power applied to port 2 couples into the secondary winding of T_2 and flows around the external loop comprising the two 50-ohm load resistors at ports 3 and 4, half the power going into each load. For the junction configuration shown, e_4 is in phase with e_2, and e_3 is 180 deg out of phase. The voltages at A and B are the same. Thus, no current flows through T_1, providing isolation at port 1 from signals into port 2. The 50-ohm port 3 and port 4 external load resistances in series present a 100-ohm load across the T_2 winding. This transforms by the square of the T_2 turns ratio $(1/2^{1}/2)^2$ to 50 ohms, matching the port 2 source.

Next, power is applied only to port 3. At port 1, the 50-ohm external load resistance is transformed by the square of the T_1 turns ratio $(1/2^{1}/2)^2$ to an effective secondary winding input resistance value R (shown dotted) of 25 ohms. Similarly, the port 2 load resistance is transformed through half of the T_2 winding by the turns ratio squared $(2^{1}/2/2)^2$ to R_b = 25 ohms. The voltage applied at port 3 divides equally across R_a and R_b, and an equal voltage is also induced across the other half of the T_1 transformer tapped winding from points B to C. This puts points A and C at the same potential; no current flows to the port 4 load, and therefore port 4 is isolated from



(a) 4-PORT, WITH EXTERNAL TERMINATIONS



(b) 3-PORT, WITH EXTERNAL/INTERNAL TERMINATIONS

Figure B-6. Four- and Three-Port Hybrid Junction Schematics

port 3. The transformer secondary input resistances of 25 ohms each for R and R_b add in series to match the 50-ohm source impedance of port 3. The power into port 3 splits equally across the transformer input resistances R and R, and therefore couples 3 db down to ports 1 and 2. With the winding sense as shown, e_3 is in phase with e_1 and both are 180 deg out of phase with e_2. For power input to port 4 only, circuit symmetry results in comparable relations to the port 3 analysis, including isolation of port 3, except that e_4, e_1, and e_2 are all in phase.

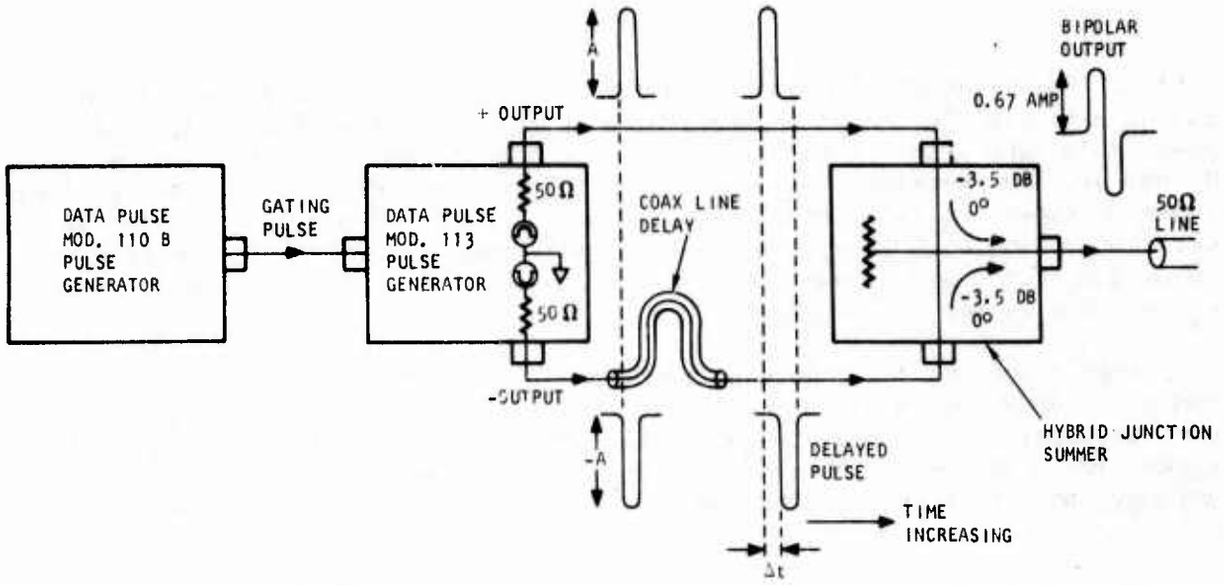
When a driven port produces two in-phase adjacent port outputs, it is a sum port (Greek letter Σ) -- port 1 or port 4 in Figure B-6. When a driven port produces 0- and 180-deg adjacent output phases, it is a difference port (Greek letter Δ) -- as for port 2 or port 3. From waveguide hybrid junction analogy, port 1 is also called the H (or symmetric) port; ports 3 and 4 the colinear ports, and port 2 the E (or antisymmetric) port.

Most of the hybrid junction devices utilized during the AiResearch duplex link investigation were 3-port dividers/summers derived from the 4-port hybrid. Where access to the antisymmetric port is not required, one transformer winding can be eliminated and one terminating load can be enclosed inside the package. The schematic for this is shown in Figure B-6b. The 50-ohm load resistance for the antisymmetric port transforms back to 100 ohms by the square of the T_2 turns ratio in Figure B-6a. A 100-ohm resistor across the tapped T_2 winding functionally replaces the other T_2 winding and the external 50-ohm load. The 100 ohms across the full winding transforms down to the 25-ohm equivalent resistances R_b and R_c, and the same analysis holds for the remaining ports as for those in the 4-port device.

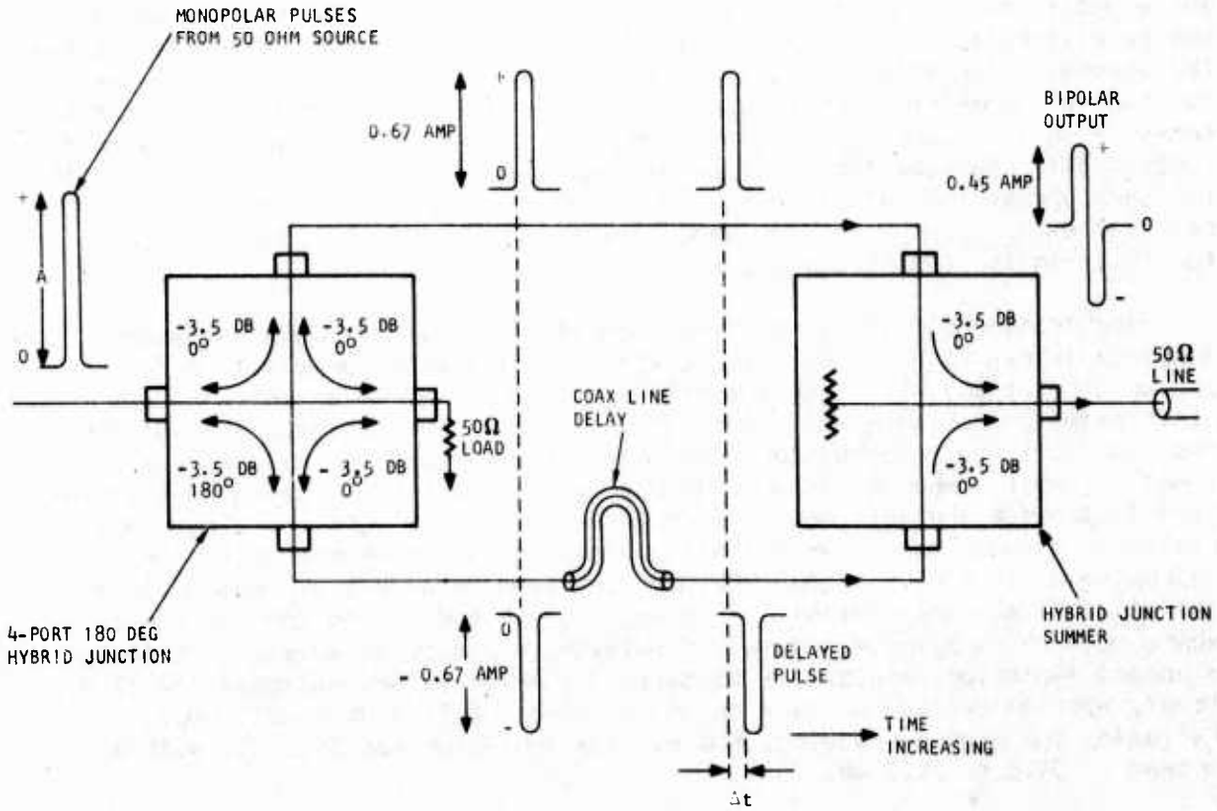
The transformer hybrid junction operation discussed above is based upon completely ideal transformer characteristics with perfect turn ratios and absence of any other performance-degrading packaging effects such as distributed capacitance and inductance. To obtain a realistic feeling for the practical isolation performance obtainable in the 1/8 in. flatpack junctions, a small number of 3-port, 3-db power dividers was obtained and isolation figure measurements made. From three vendors, a total of eleven power divider flatpacks was obtained, all having bandpasses encompassing the approximate range of 5 to 500 mHz and specified to have a minimum of 30 db isolation at any point within the bandpass. In the 180 to 200 mHz range, where good correlation was obtained between cw and pulse waveform (5 nsec, bipolar) isolation values, all measured isolation values exceeded the 30 db level, with an average of 38.4 db and a spread of 31.5 db to 77.5 db. Excluding the highest reading, the average isolation was 34.5 db, with a spread of 31.5 to 39.2 db.

9. BIPOLAR PULSE TEST SOURCES FOR THE DUPLEXER

The test signals utilized in the AiResearch full-duplex data link investigation were required to be bipolar to avoid dc baseline shifts occurring with long sequences of monopolar pulses. Two methods were developed to convert the pulses generated by the Datapulse 113 into bipolar form. The first, as shown in Figure B-7a, utilized the complementary positive and negative pulse output feature of the 113 pulse generator. The generator was adjusted for pulse



(a) UTILIZING COMPLEMENTARY PULSE SOURCE



(b) UTILIZING MONOPOLOR PULSE SOURCE

Figure B-7. Bipolar Test Pulse Generating Sources

duration of about 3 nsec and 200-megabit repetition rate. Both complementary pulse outputs were then coupled into the matching 50-ohm colinear ports of a transformer hybrid junction with 50-ohm coaxial transmission line. The length of one line (either one for test purposes) was trimmed longer than the other to provide a 2.5-nsec differential delay in time of arrival at the hybrid junction. The three desired results were then realized at the junction: (1) 50-ohm impedance matching to the lines at all three ports, (2) greater than 30 db of isolation between the two pulse generator outputs across the two colinear ports, and (3) summing of the two opposite polarity pulses to produce 5-nsec duration bipolar pulses. Pulse groups containing from one to ten bipolar pulses at 200 megabit/sec were then controlled by the gating pulse generator.

For generating bipolar pulses from monopolar pulse sources, the same delay and summing arrangement described above can be utilized, but with the complementary pulses generated from monopolar pulses by a passive 4-port, 180-deg hybrid junction (as shown in Figure B-7b). The 180-deg hybrid is similar to the hybrid junction divider/summer, the fourth (antisymmetric) port being brought out rather than internally terminated. As shown, a signal into the antisymmetric port is split equally between the two adjacent ports, in phase at one and inverted 180 deg at the other, thus providing complementary pulse outputs from a monopolar pulse input.

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